Hades_840M_ULT
Schematics Document

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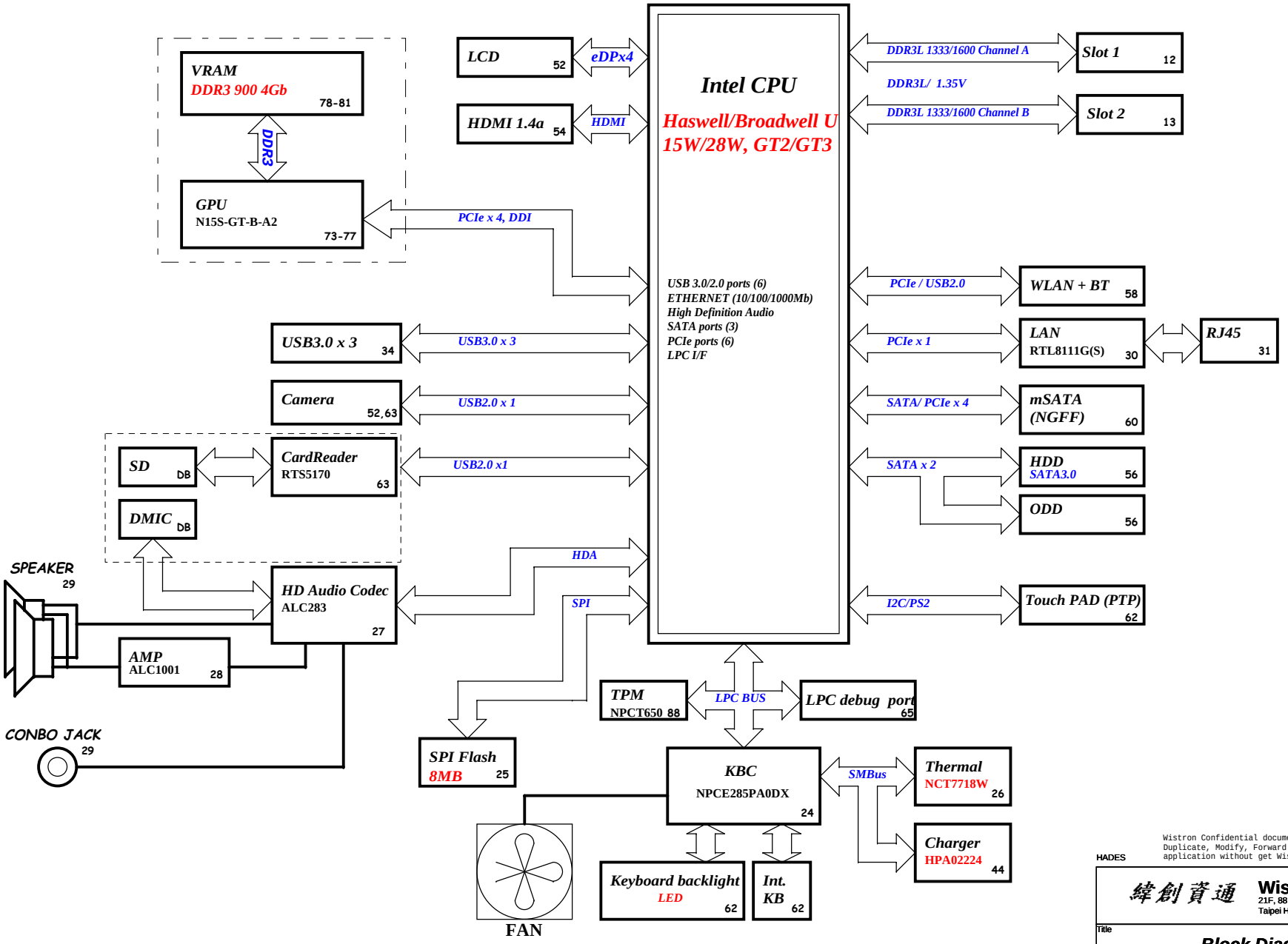
Title: ***Cover Page***

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 1 of 102

Hades ULV Board Block Diagram

Project code : 4PD02F010001
PCB P/N : 14205
Revision : -1



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Title: Block Diagram

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

Date: Thursday, May 22, 2014 | Sheet 2 of 102

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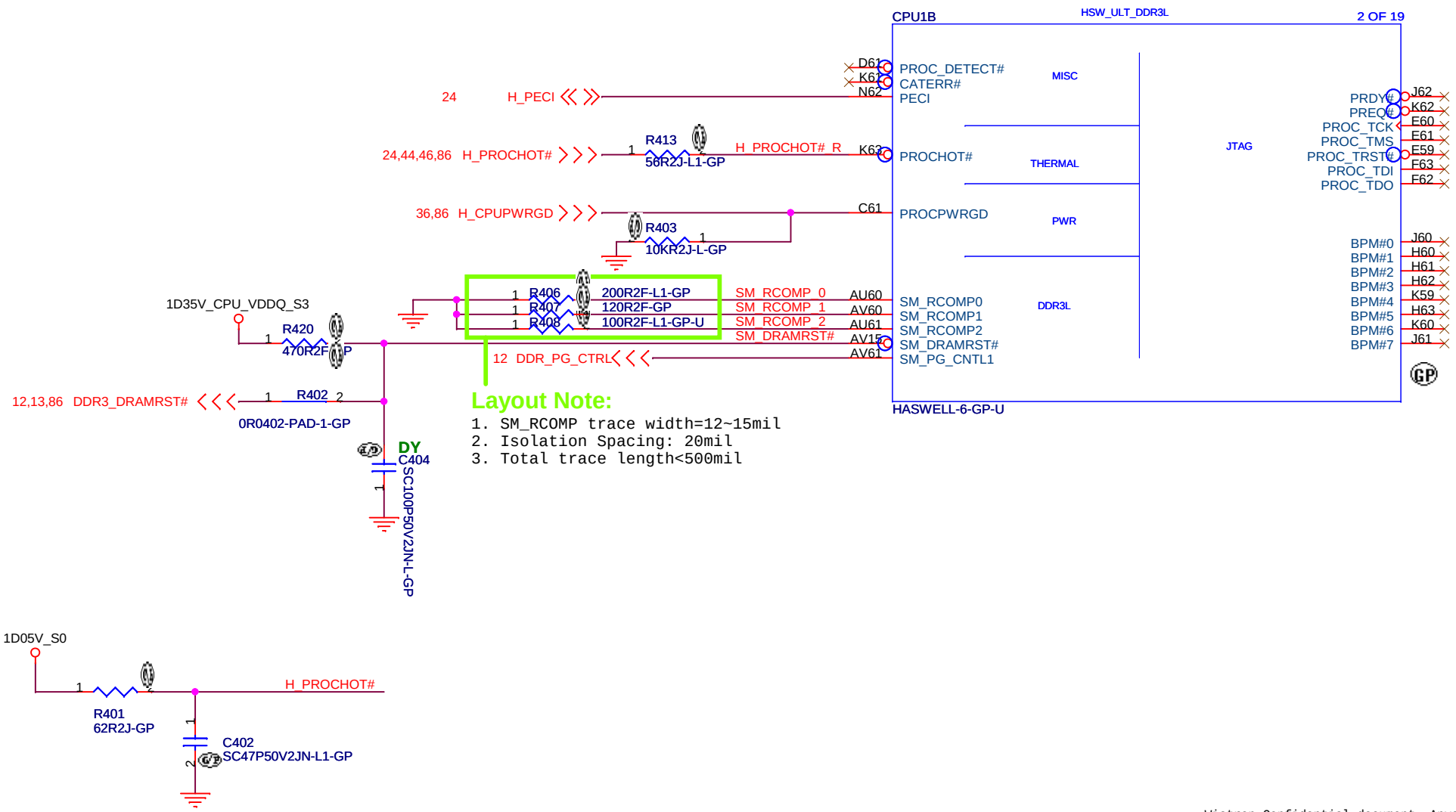
Title

CPU (Reserved)

Size	Document Number	Rev
A4	**Hades_840M_ULT**	**-1**

Date: Wednesday, April 30, 2014 Sheet 3 of 102



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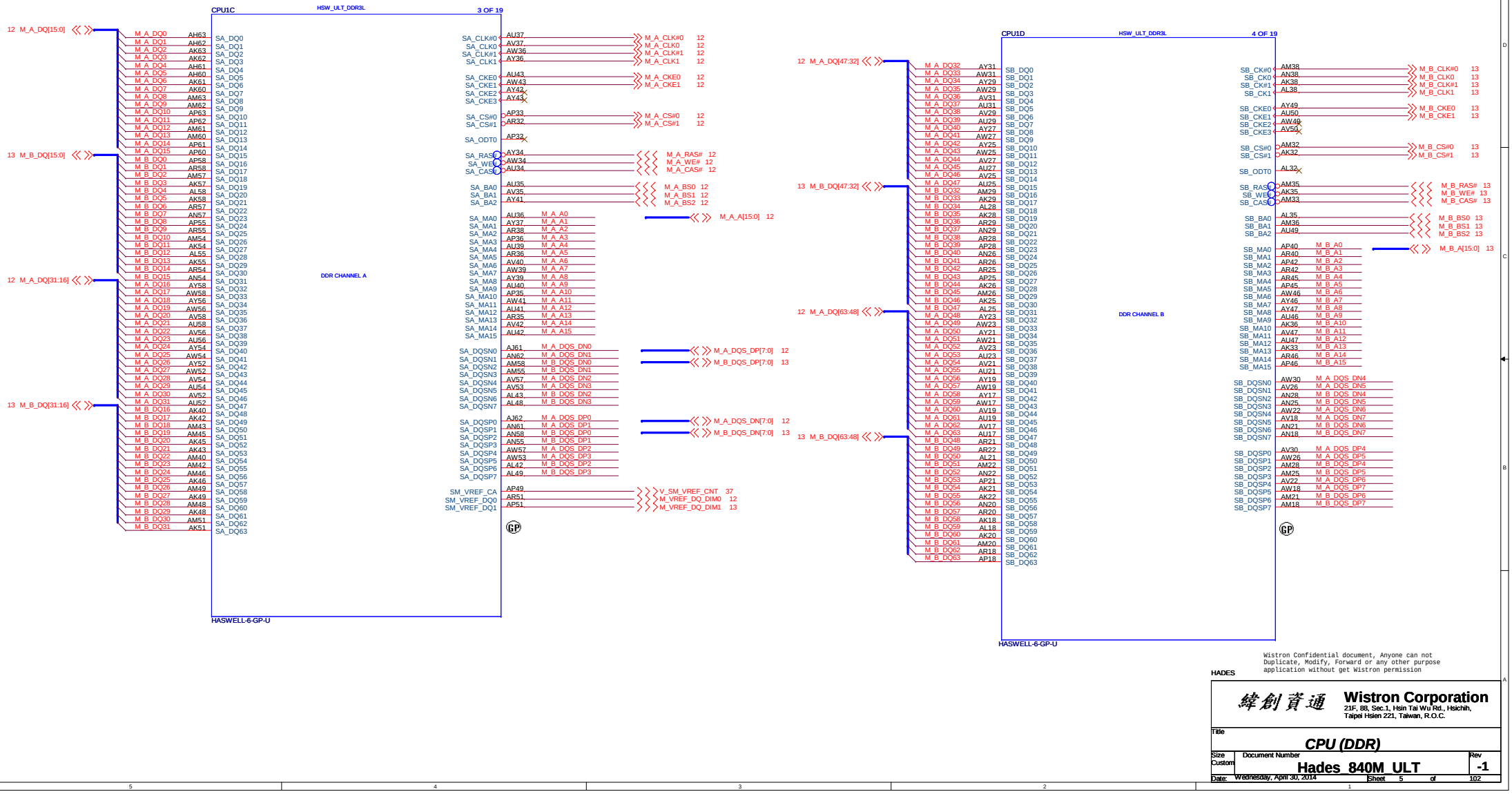
Title
CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 4 of 102

SSID = CPU



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Title: **CPU (DDR)**

Size	Document Number	Rev
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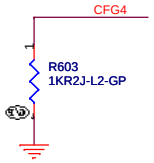
Date: Wednesday, April 30, 2014 Sheet 5 of 102

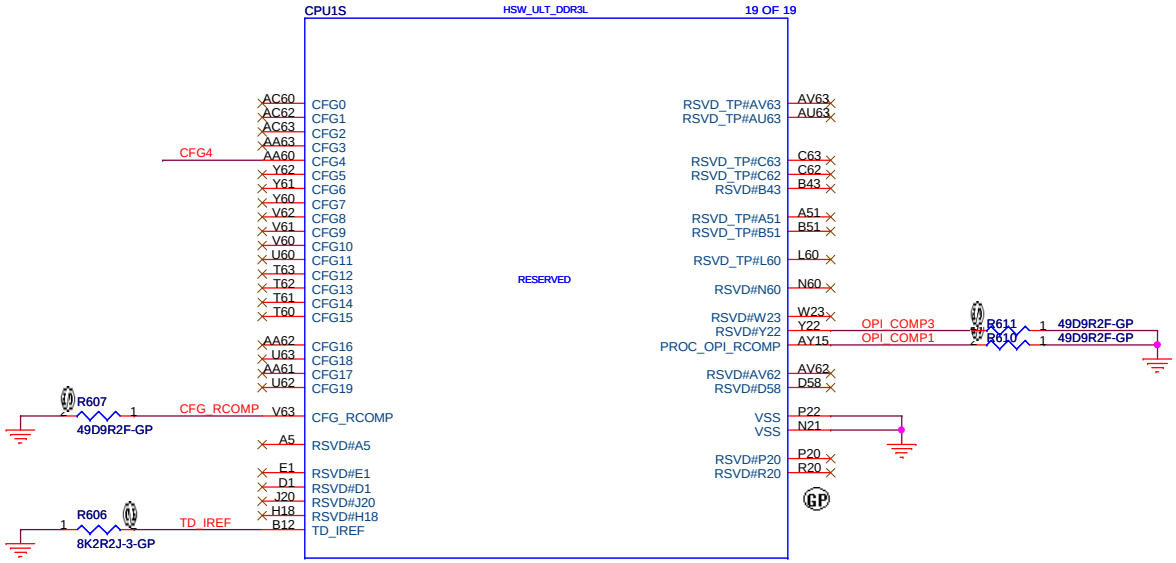
SSID = CPU

Pin Name	System Pull-up/Pull-down	Schematic Notes	✔
CFG[19:0]		Please refer to the *Crescent Bay and (??) Platforms - Debug Port Design Guide (DPDG)* .	

Note: Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

eDP Enable	
CFG4	1:Disable
	0:Enable





Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[3:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • PCI Express* Static x16 Lane Numbering Reversal. — — • • **CFG[4]: eDP enable** — 1 = Disabled — 0 = Enabled • **[19:5]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	

continued...

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

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Title: **CPU (CFG)**

Size: Custom | Document Number: **Hades_840M_ULT** | Rev: **-1**

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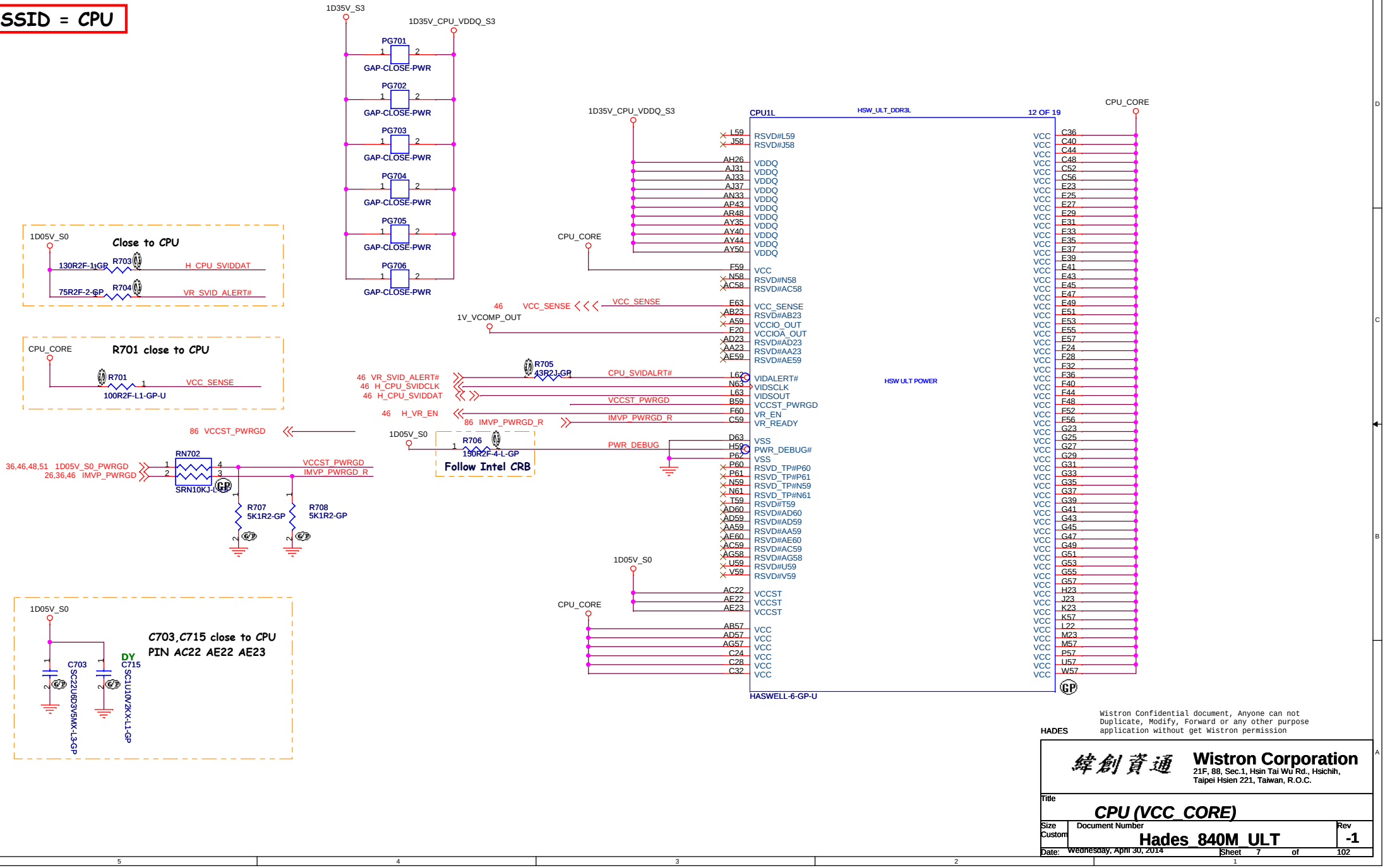
SSID = CPU



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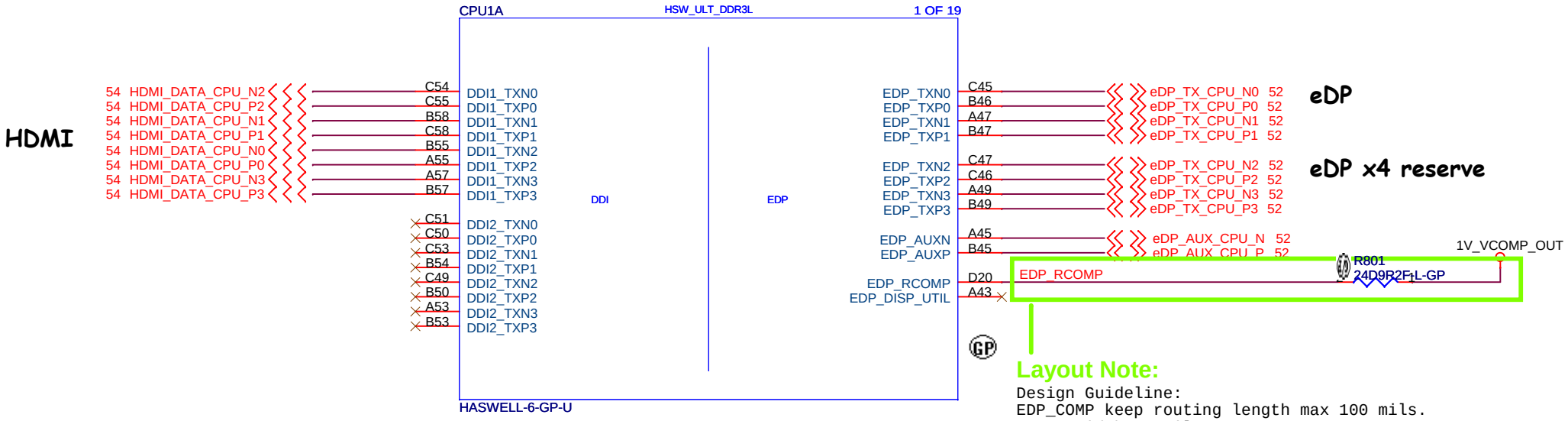
Title: CPU (VCC_CORE)

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 7 of 102

SSID = CPU



Layout Note:

Design Guideline:
EDP_COMP keep routing length max 100 mils.
Trace Width:20 mils.

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

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Title: ***CPU (DDI/EDP)***

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

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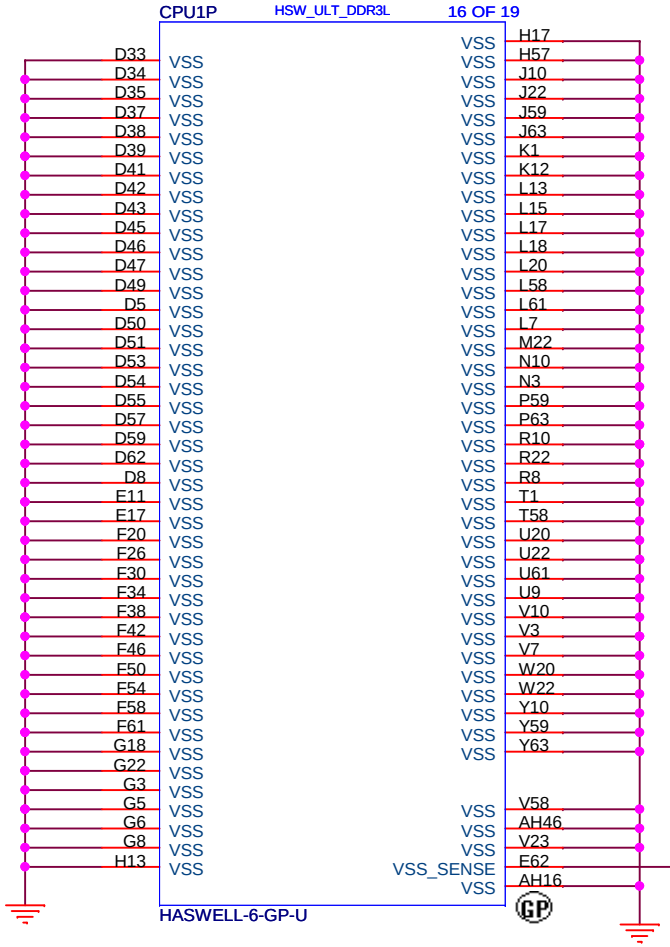
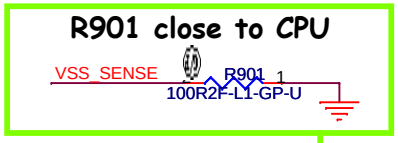
SSID = CPU





VSS_SENSE 46

Layout Note:

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Title: CPU (VSS)

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

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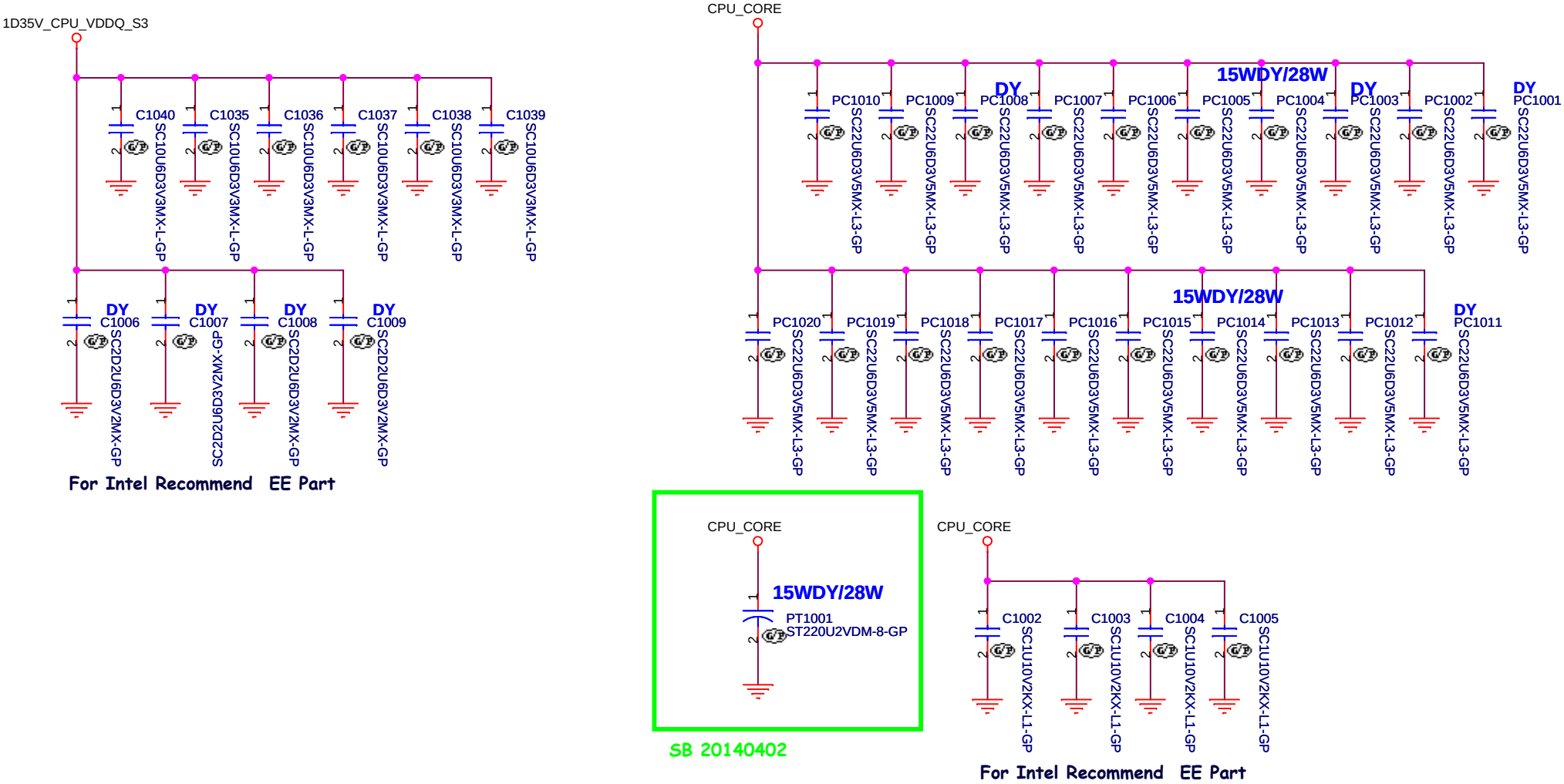

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Title: **CPU (Power CAP1)**

Size	Document Number	Rev
A4	Hades 840M ULT	-1

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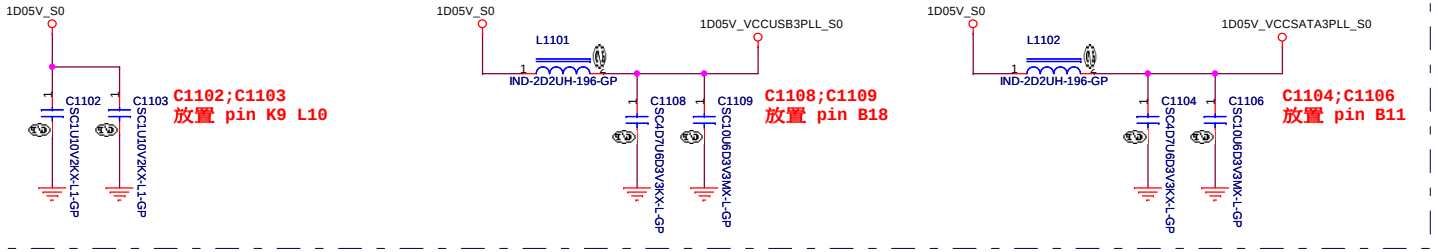
擺放電容的位置請參考 Page 21,每個位置如下

MAX: 1.92A



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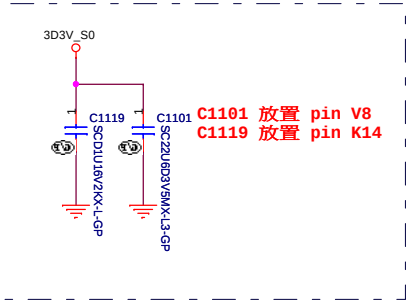

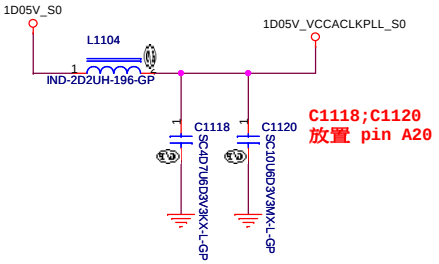

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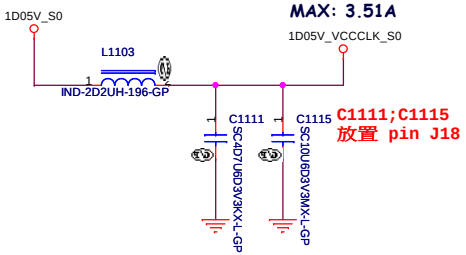

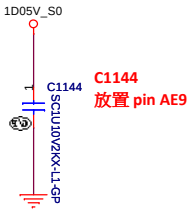

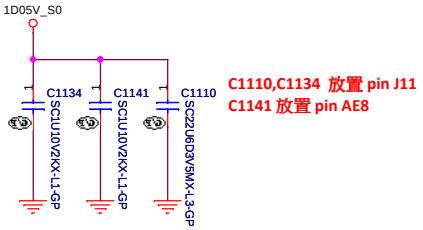

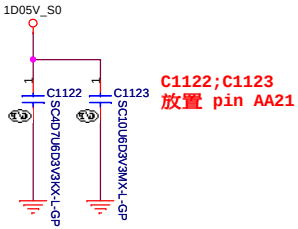

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Title: CPU (Power CAP2)

Size: Custom | Document Number: Hades 840M ULT | Rev: -1

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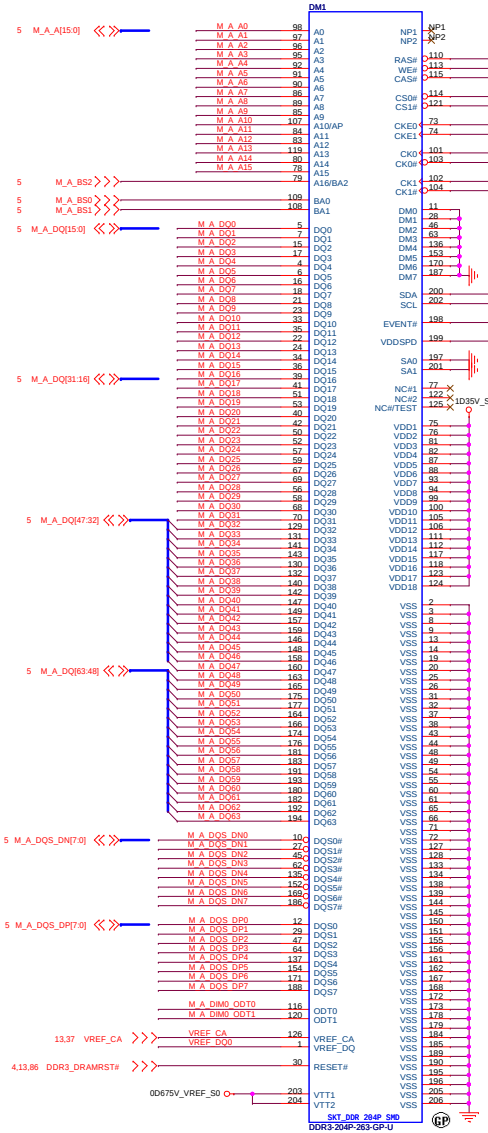
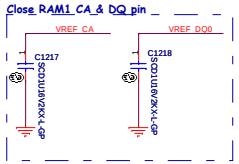
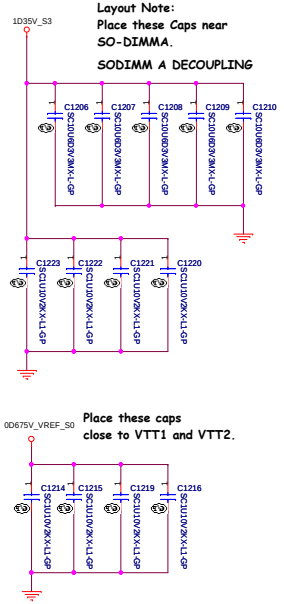
SSID = MEMORY





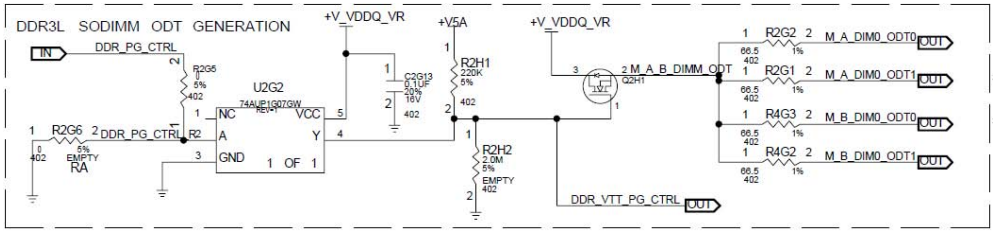


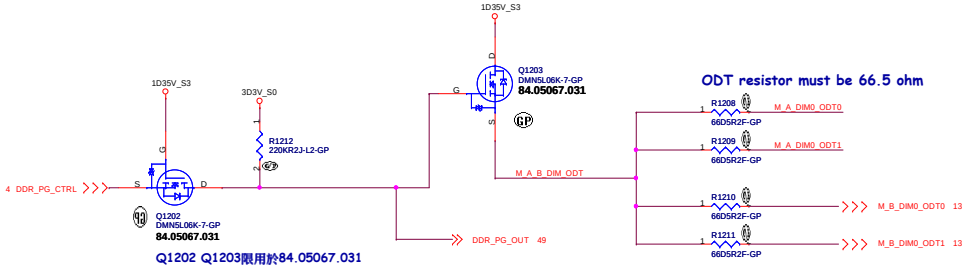
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

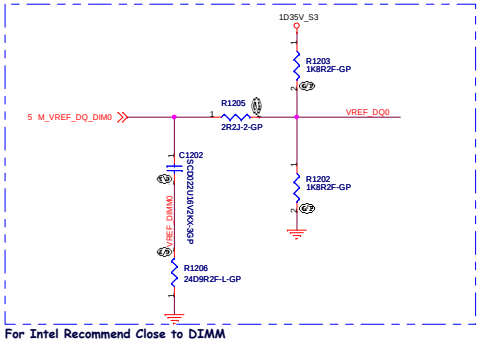
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SODIMM Memory Connectivity and Topology
ODT Signal Connectivity and Support
For DDR3L SODIMM designs, Intel recommends ODT signals not to be routed between CPU and DIMM on platform, leave ODT at CPU as no-connect (open), and tie DIMM ODT to VDDQ through FET and resistor. The reason for this additional ODT-control circuitry on the platform is to save power dissipation by turning off VDDQ to VTT path during low power states, as ODT signal is terminated to VTT through RTT on SODIMM. The ODT value for DDR3L SODIMM 1-DPC platform will be encoded in the write command and use RTT_NOM = Off and RTT_WR = (60,120) Ohm.

- CPU ODT output would be NOCON
- SODIMM ODT input should be tied to VDDQ through a FET and a resistor to support low power states.







For Intel Recommend Close to DIMM

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Title: **DDR3-SODIMM1**

Size	Document Number	Rev
A2	Hades_840M_ULT	-1

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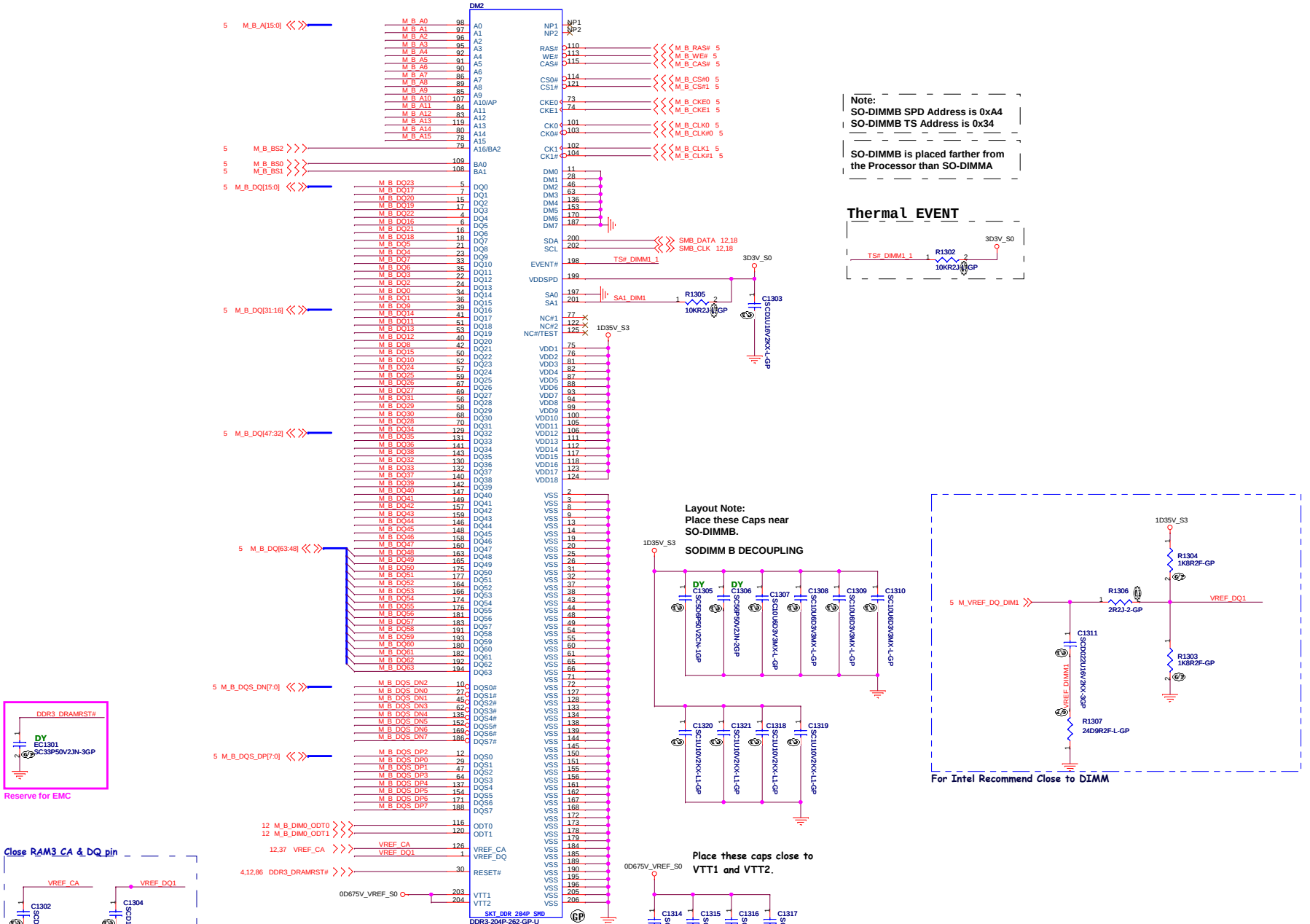
SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

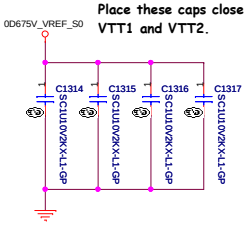
SO-DIMMB is placed farther from the Processor than SO-DIMMA

Thermal EVENT

Layout Note:
Place these Caps near SO-DIMMB.

SODIMM B DECOUPLING

Place these caps close to VTT1 and VTT2.



For Intel Recommend Close to DIMM

Reserve for EMC

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Title: DDR3-SODIMM2

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

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Title

(Reserved)_SODIMM_SODIMM4

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A4	Hades_840M_ULT	-1
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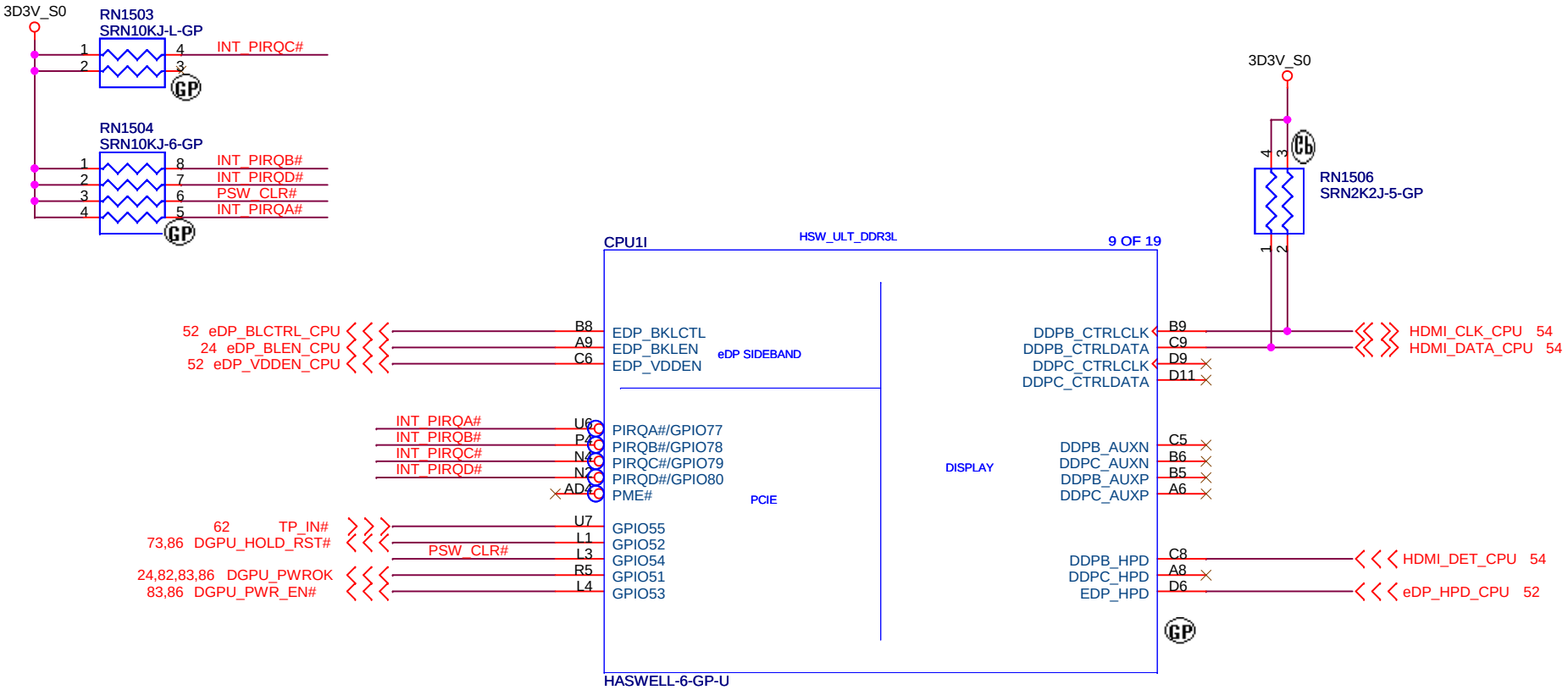

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Title
CPU(EDP SIDEBAND/GPIO/DDI)

Size	Document Number	Rev
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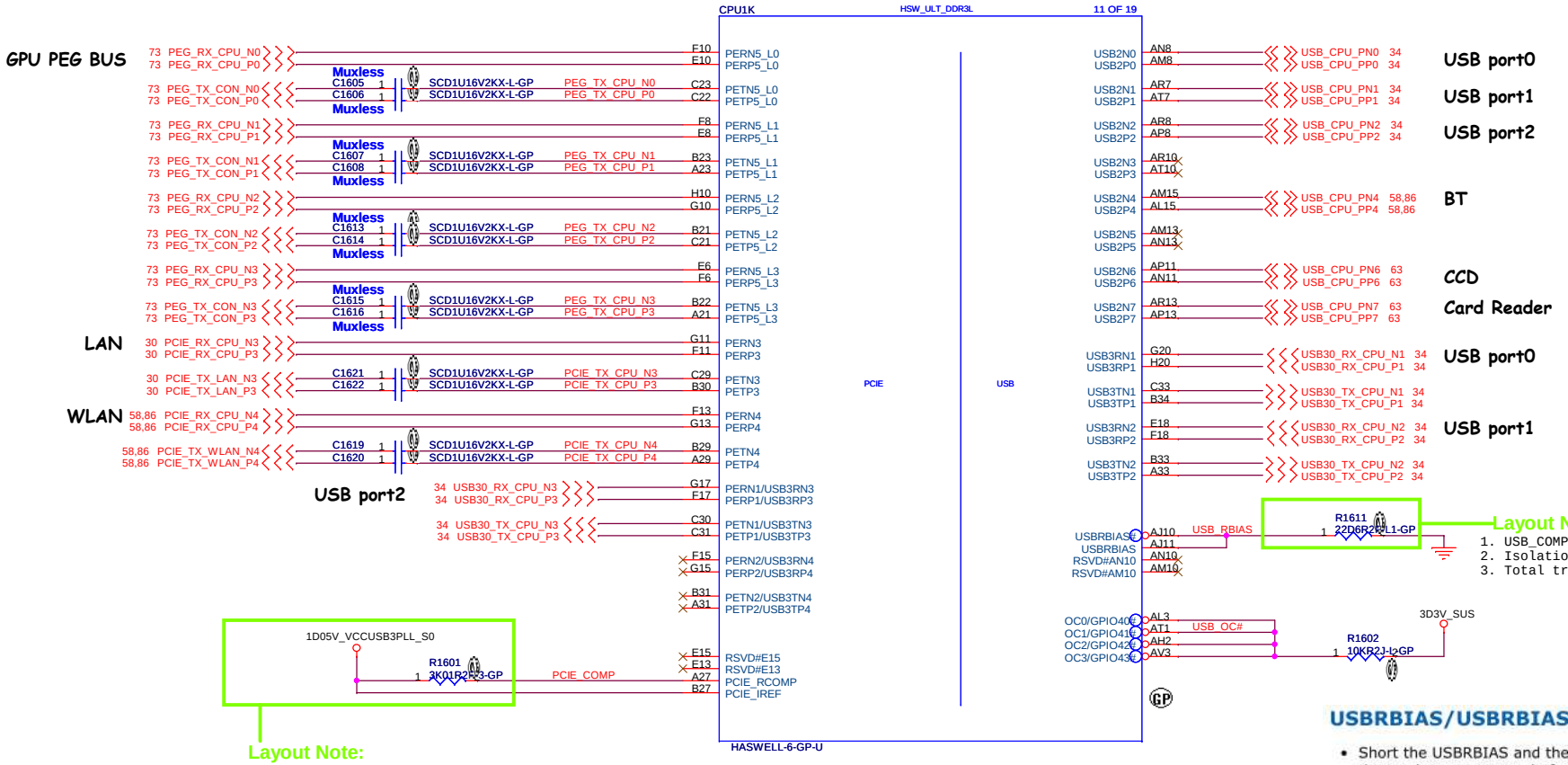

USB Table

Pair	Device
0	USB3.0 Port0
1	USB3.0 Port1
2	USB3.0 Port3
3	
4	BT
5	
6	CCD
7	Card Reader

Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

USBRBIAS/USBRBIAS# Connection Guidelines

- Short the USBRBIAS and the USBRBIAS# pins at the package and then route on the top layer to one end of a 22.6 Ω ±1% resistor to ground (see Figure 15-2).
- Route signal using 50 ohm single-ended impedance and 500 mils (12.7-mm) max trace length and no longer than 450 mils to resistor.
- Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 15 mils (0.381 mm).

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

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Title: CPU (PCI/USB)

Size: A3 | Document Number: Hades 840M ULT | Rev: -1

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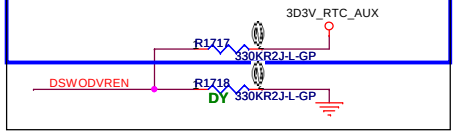
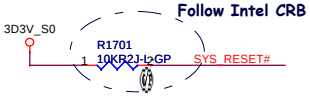
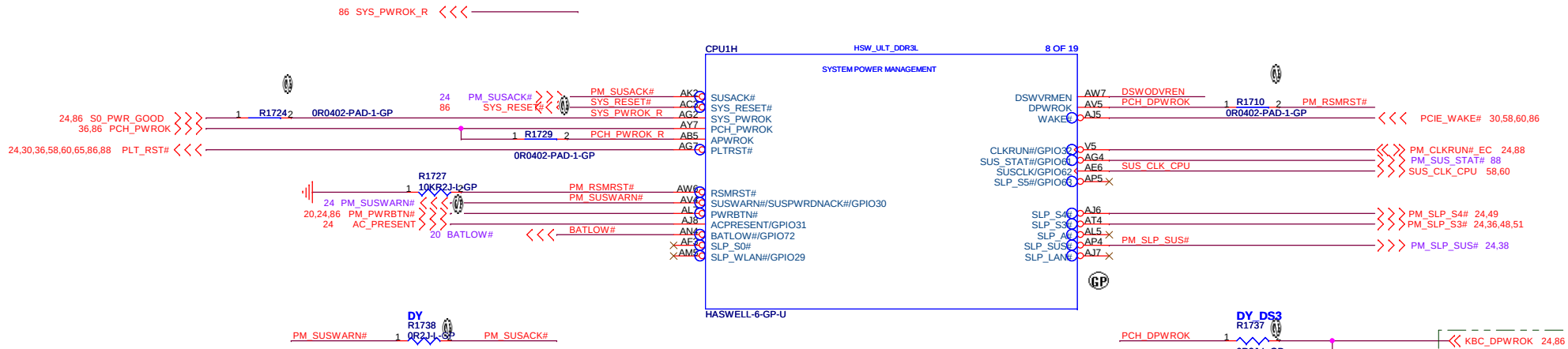
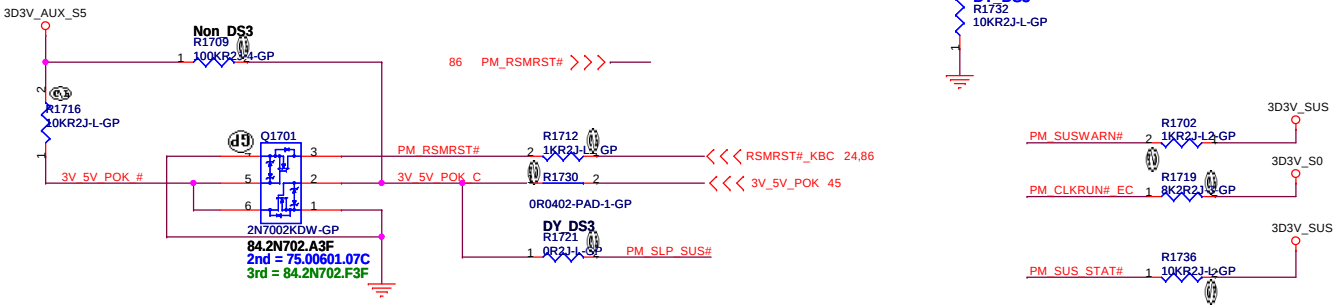
Bit	Description
31:3	Reserved
2	**WAKE# Pin Deep Sx Enable (WAKE_PIN__DSX_EN)** - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0': • Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. • Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. **NOTE:** Deep Sx disabled configuration must leave this bit at '0'.

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

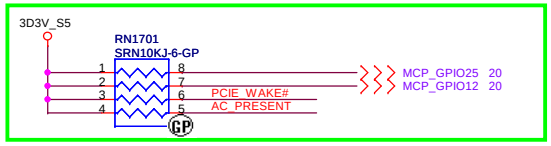








SB 20140402



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Title: **CPU (DMI/FDI/PM)**

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close to PCH

3D3V_S0

RN1808 SRN10KJ-6-GP
1 PEG_CLKREQ_CPU#
2 LAN_CLKREQ_CPU#
3 WLAN_CLKREQ_CPU#
4 CK_REQ

R1805 10KR2J-L-GP
MSATA_CLKREQ_CPU#

CPU1F HSW_ULT_DDR3L 6 OF 19

CK_REQ
C43 CLKOUT_PCIE_N0
C42 CLKOUT_PCIE_P0
U2 PCIECLKRQ0#/GPIO18

CK_REQ
B41 CLKOUT_PCIE_N1
A41 CLKOUT_PCIE_P1
Y5 PCIECLKRQ1#/GPIO19

C41 CLKOUT_PCIE_N2
B42 CLKOUT_PCIE_P2
AD1 PCIECLKRQ2#/GPIO20

B38 CLKOUT_PCIE_N3
C37 CLKOUT_PCIE_P3
N1 PCIECLKRQ3#/GPIO21

A39 CLKOUT_PCIE_N4
B39 CLKOUT_PCIE_P4
U5 PCIECLKRQ4#/GPIO22

B37 CLKOUT_PCIE_N5
A37 CLKOUT_PCIE_P5
T2 PCIECLKRQ5#/GPIO23

HASWELL-6-GP-U

CLOCK SIGNALS

XTAL24_IN A25 CPU_XTAL_24M_IN
XTAL24_OUT B25 CPU_XTAL_24M_OUT

RSVD#K21 K21
RSVD#M21 M21
DIFFCLK_BIASREF C26 DIFFCLK_BIAS

R1801 3K01R2F-3-GP
1D05V_VCCACLKPLL_S0

TESTLOW_C35 C35 CLK_BUF_CKSSCD_N
TESTLOW_C34 C34 CLK_BUF_CKSSCD_P
TESTLOW_AK8 AK8 CLK_BUF_DOT96_P
TESTLOW_AL8 AL8 CLK_BUF_DOT96_N

R1804 22R2J-2-GP
CLK_PCI_LPC 65,86

CLKOUT_LPC_0 AN15 CLK_PCI_LPC_R
CLKOUT_LPC_1 AP15 CLK_PCI_TPM_R

R1803 22R2J-2-GP
CLK_PCI_KBC 24,86
CLK_PCI_TPM 86,88

R1802 22R2J-2-GP

CLKOUT_ITPXDP# B35
CLKOUT_ITPXDP_P A35

Need very close to PCH

RN1810 SRN10KJ-L-GP
CLK_BUF_CKSSCD_N
CLK_BUF_CKSSCD_P

RN1811 SRN10KJ-L-GP
CLK_BUF_DOT96_P
CLK_BUF_DOT96_N

CPU_XTAL_24M_IN
C1808 SC15P50V2JN-L-GP
X1801 XTAL-24MHZ-81-GP 82.30004.841
R1807 1MR2J-L3-GP
CPU_XTAL_24M_OUT
C1807 SC15P50V2JN-L-GP

CPU1G HSW_ULT_DDR3L 7 OF 19

LPC
24,65,88 LPC_AD_CPU_P0 AU14 LAD0
24,65,88 LPC_AD_CPU_P1 AW12 LAD1
24,65,88 LPC_AD_CPU_P2 AY12 LAD2
24,65,88 LPC_AD_CPU_P3 AW11 LAD3
24,65,88 LPC_FRAME#_CPU AV12 LFRAME#

SMBUS
SMBALERT#/GPIO11 AN2 MCP_GPIO11
SMBCLK AP2 SMB_CLK_CPU
SMBDATA AH1 SMB_DATA_CPU
SML0ALERT#/GPIO60 AL2 MCP_GPIO60
SML0CLK AN1 SML0_CLK_CPU
SML0DATA AK1 SML0_DATA_CPU
SML1ALERT#/PCHHOT#/GPIO73 AU4 MCP_GPIO73
SML1CLK/GPIO75 AU3
SML1DATA/GPIO74 AH3
SML1_CLK 24,26,76
SML1_DATA 24,26,76
MCP_GPIO73 20
EC / Therma/ VGA

SPI
24,25 SPI_CLK_CPU AA3 SPI_CLK
24,25 SPI_CS_CPU_N0 Y2 SPI_CS0#
Y1 SPI_CS1#
AC2 SPI_CS2#
24,25 SPI_SI_CPU AA2 SPI_MOSI
24,25 SPI_SO_CPU AA4 SPI_MISO
25 SPI_WP_CPU Y6 SPI_IO2
25 SPI_HOLD_CPU AF1 SPI_IO3

C-LINK
CL_CLK AF2
CL_DATA AD2
CL_RST# AF4

HASWELL-6-GP-U

3D3V_SUS

RN1803 SRN2K2J-5-GP
SMB_CLK_CPU
SMB_DATA_CPU

R1808 2K2R2J-2-GP
SML0_DATA_CPU

R1809 2K2R2J-2-GP
SML0_CLK_CPU

R1810 2K2R2J-2-GP
SML1_CLK

R1811 2K2R2J-2-GP
SML1_DATA

3D3V_S0

RN1807 SRN2K2J-5-GP

Q1801 2N7002KDW-GP
84.2N702.A3F
2nd = 75.00601.07C
3rd = 84.2N702.F3F
SMB_DATA_CPU
SMB_DATA 12,13
SMB_CLK_CPU
SMB_CLK 12,13

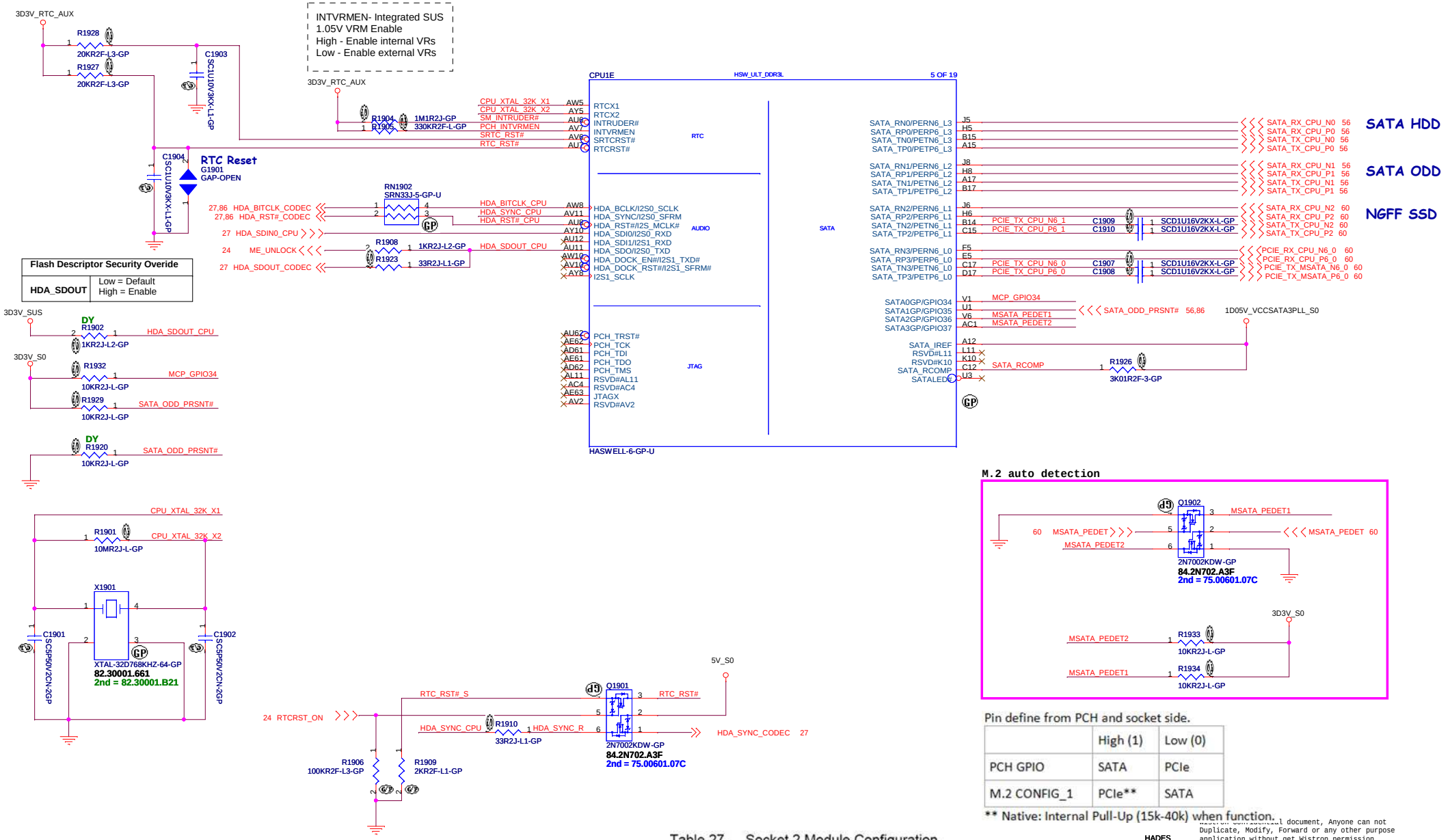
3D3V_SUS

RN1804 SRN10KJ-6-GP
MCP_GPIO60
MCP_GPIO11
MCP_GPIO13
MCP_GPIO8
20 MCP_GPIO13
20 MCP_GPIO8

HADES

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCI-E/SMBUS/CLOCK/CL)
Size: A3 Document Number: Hades_840M_ULT Rev: -1
Date: Wednesday, April 30, 2014 Sheet 18 of 102



Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

HADES

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RTC/LPC/SATA/HDA)

Size: Custom | Document Number: Hades 840M ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 19 of 102

SB 20140428

SB 20140402

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

[DGPU_TYPE1:DGPU_TYPE2]
HH:UMA LL=840
HL:850 LH=reserve

	GSPIO_MOSI_BBSO_R(SSD_PWR)
PU	RESERVED
PD	SPI BUS

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Taipei Hsien 221, Taiwan, R.O.C.

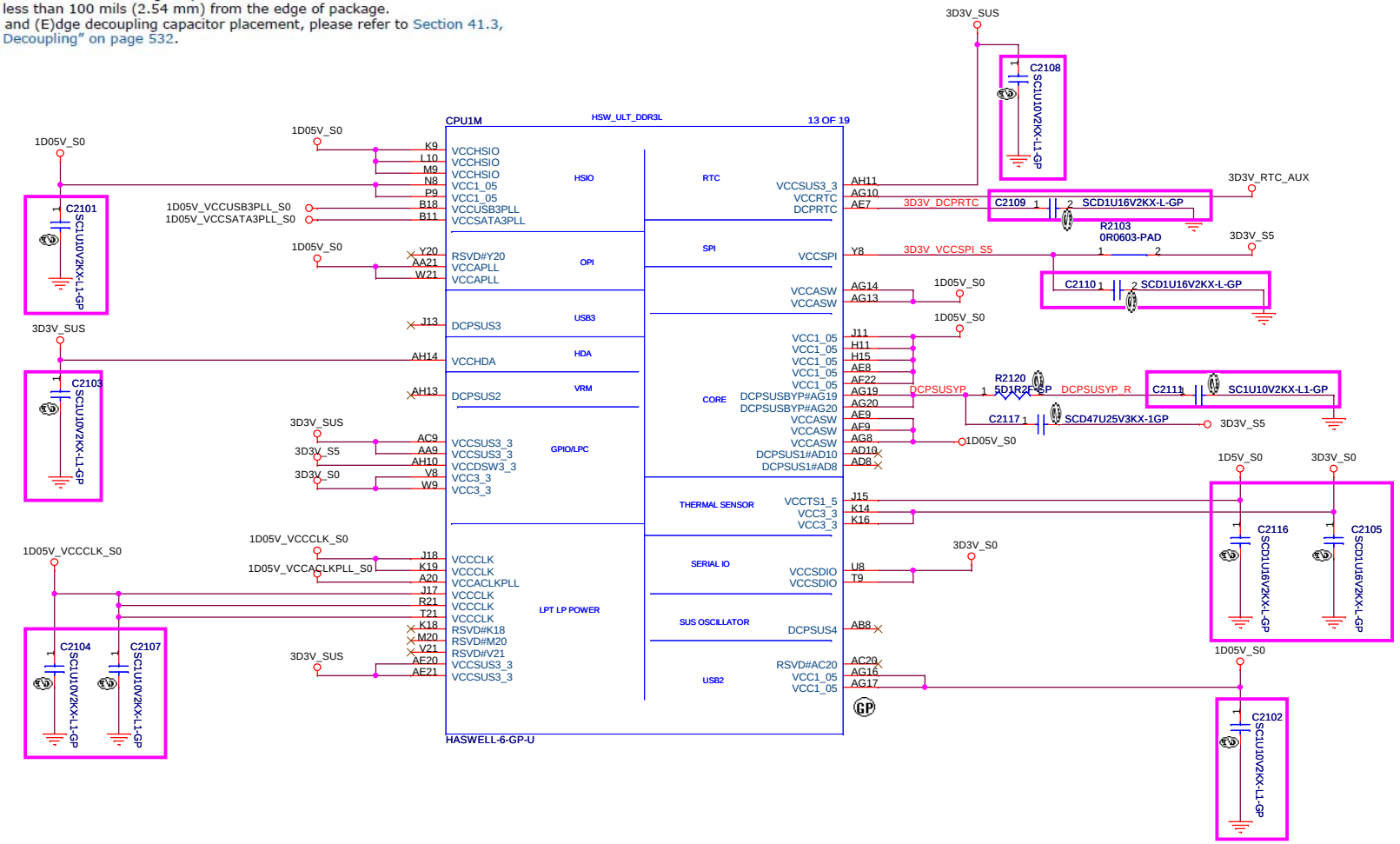
Title: CPU (GPIO/MISC)

Size: A3 | Document Number: Hades 840M ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 20 of 102

Notes:

1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to Section 41.3, "Loop Inductance Reduction Decoupling" on page 532.



HADES

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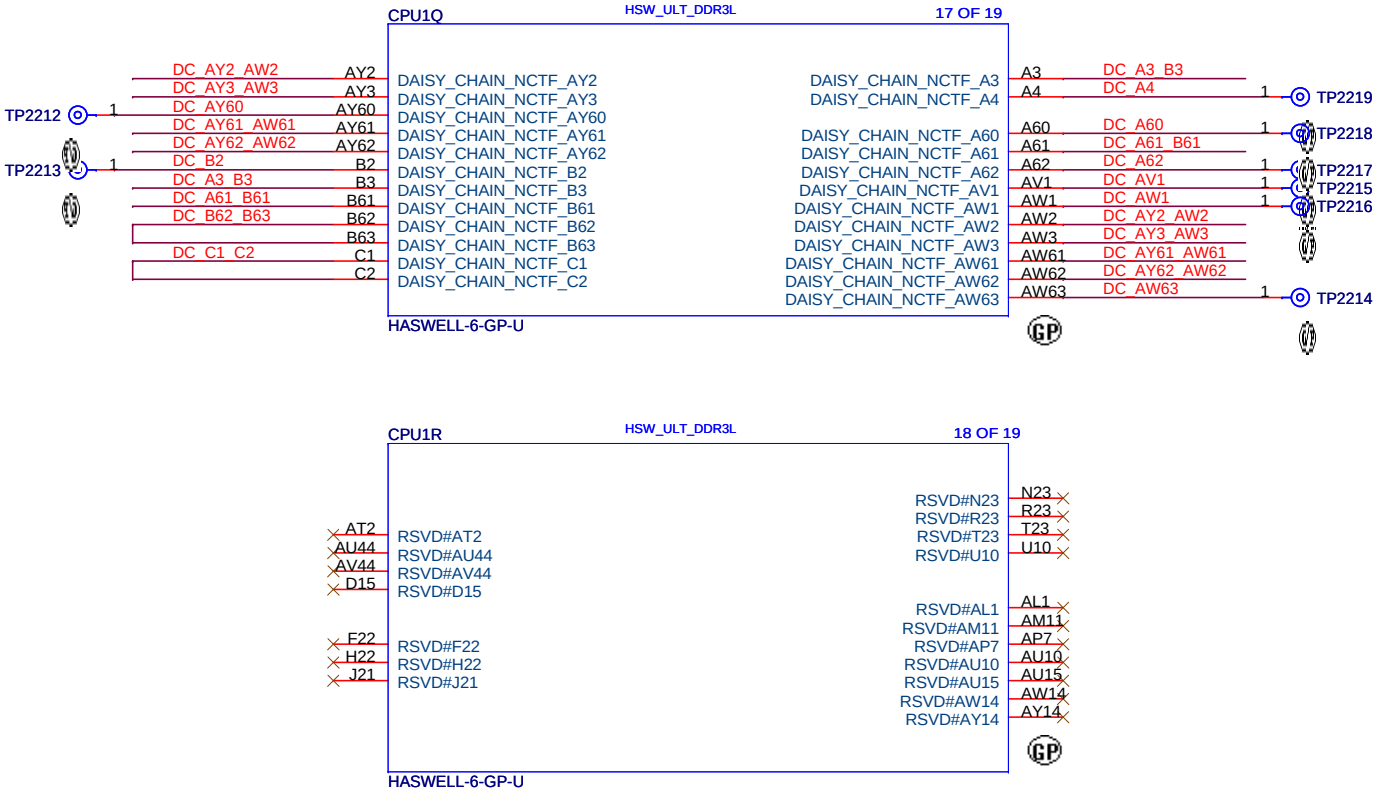
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (POWER1)**

Size	Document Number	Rev
A3	Hades 840M ULT	-1

Date: Wednesday, April 30, 2014 Sheet 21 of 102



HADES

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (RSVD)

Size	Document Number	Rev
Custom	Hades_840M_ULT	-1
Date: Wednesday, April 30, 2014	Sheet 22 of 102	

HADES

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 23 of 102

SSID = KBC

BATTER /CHARGER--->

Thermal/eDP/GPU--->

Touch Pad--->

20K : 64.20025.L0L

GPIO0 High Active

2ND = 84.T3906.E11

84.T3906.A11

84.2N702.J31

2ND = 84.2N702.031

2nd = 75.005V0.A7D

75.05125.07D

-1 20140514

Model_ID	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
VA30	100.0 K	10.0 K	3.000 V	3.0054	>= 2.875 V	
Hades UMA	100.0 K	20.0 K	2.750 V	2.7591	>= 2.616 V	< 2.875 V
Hades DIS 840	100.0 K	33.0 K	2.481 V	2.4935	>= 2.363 V	< 2.616 V
Hades DIS 850	100.0 K	47.0 K	2.245 V	2.2592	>= 2.123 V	< 2.363 V
Hades DIS 860	100.0 K	64.9 K	2.001 V	2.0169	>= 1.934 V	< 2.123 V
Poseidon DIS 840	100.0 K	76.8 K	1.867 V	1.8827	>= 1.758 V	< 1.934 V
Poseidon DIS 860	100.0 K	100.0 K	1.650 V	1.6665	>= 1.504 V	< 1.758 V
Poseidon DIS 850	100.0 K	143.0 K	1.358 V	1.3740	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	>= 0.524 V	< 1.126 V

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.3055	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.5592	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.8312	>= 0.684 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.0695	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.3146	>= 1.177 V	< 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.4497	>= 1.366 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.6665	>= 1.542 V	< 1.842 V

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.0054	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.7591	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2592	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	>= 0.524 V	< 1.126 V

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Title: KBC_ITE8587

Size: A2 | Document Number: Hades_840M_ULT | Rev: -1

Date: Friday, May 16, 2014 | Sheet 24 of 102

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

SPI FLASH ROM (8M byte)
1ST= 072.02564.0001(AMIC A25LQ64M)
2ND=072.25B64.0001(Gigadevice GD25B64BSIGR)

purge=72.25Q64.K01 (WINBOND W25Q64FVSSIQ)
72.25647.00A (MXIC MX25L6473EM2I)

Figure 28-1. SPI Topology (Single Device)

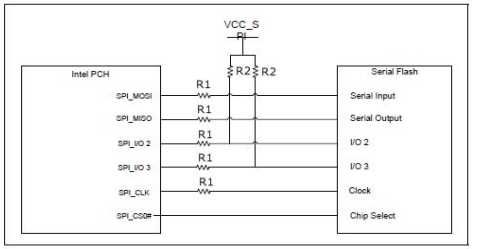
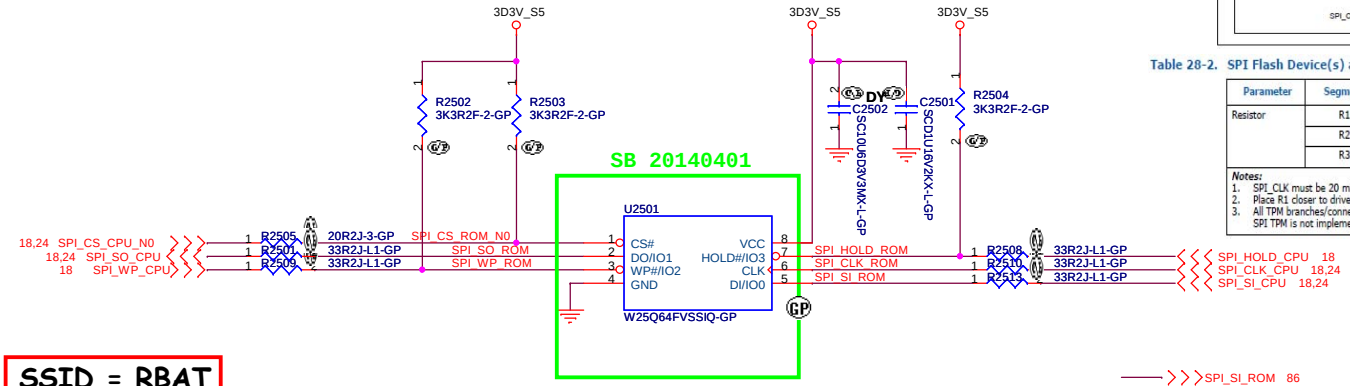


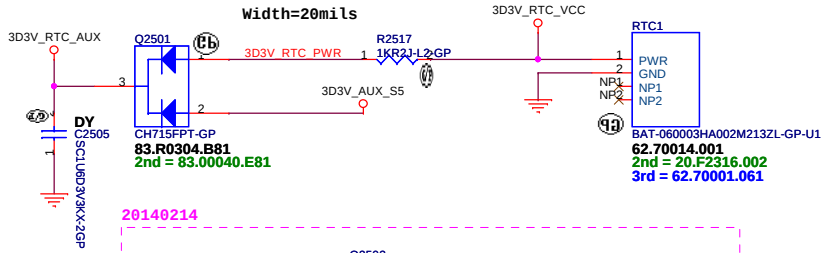
Table 28-2. SPI Flash Device(s) and TPM Routing Guideline (Sheet 2 of 2)

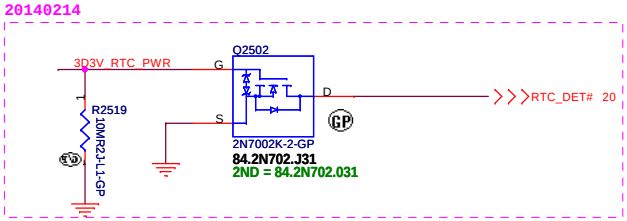
Parameter	Segment	Stackup	Unit	Routing Recommendation
Resistor	R1		ohm	15
	R2		ohm	1k
	R3		ohm	33

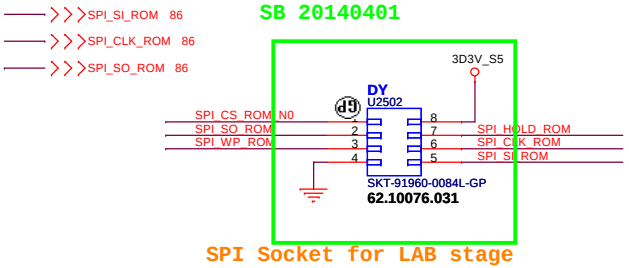
Notes:
1. SPI_CLK must be 20 mils spacing from any other high frequency (>1 GHz) signal.
2. Place R1 closer to driver side to effectively damping the undershoot and overshoot.
3. All TPM branches/connections (TPM_MOSI, TPM_MISO, TPM_CLK, and PCH_CS2#) can be left as NC if SPI TPM is not implemented.



SSID = RBAT







HADES

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Flash(KBC+PCH)/RTC***

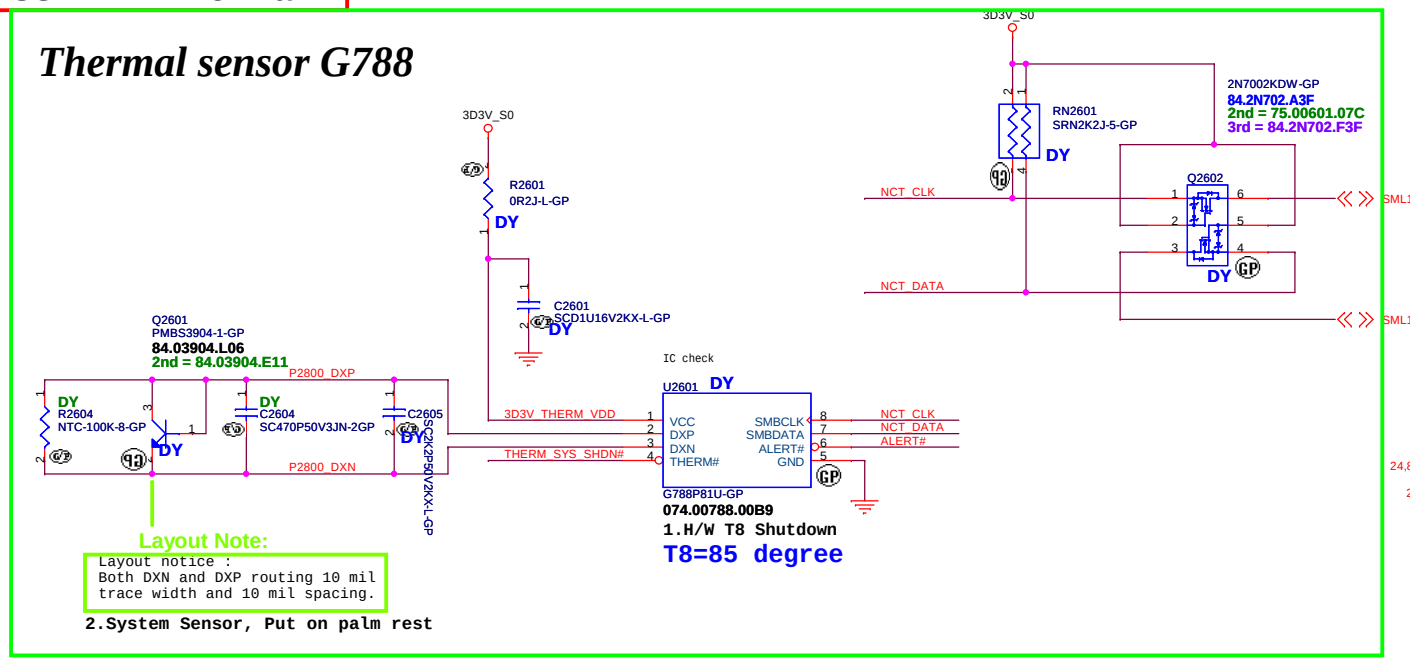
Size: A3 | Document Number: **Hades_840M_ULT** | Rev: **-1**

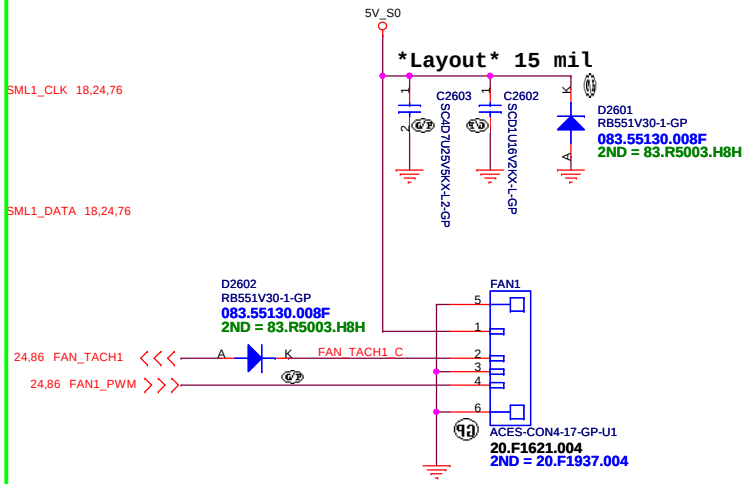
Date: Wednesday, April 30, 2014 | Sheet 25 of 102

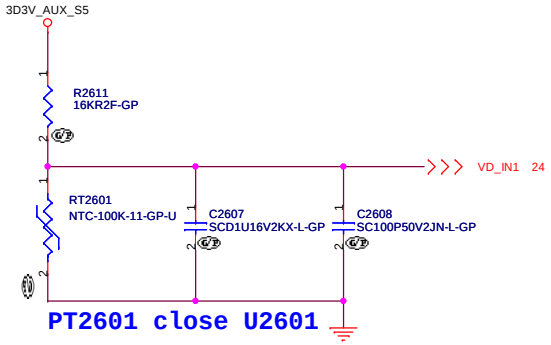
SSID = Thermal

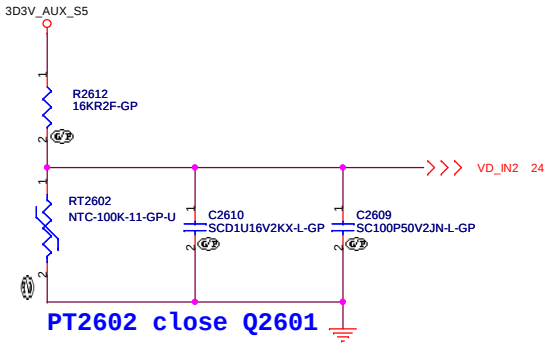
SB 20140401

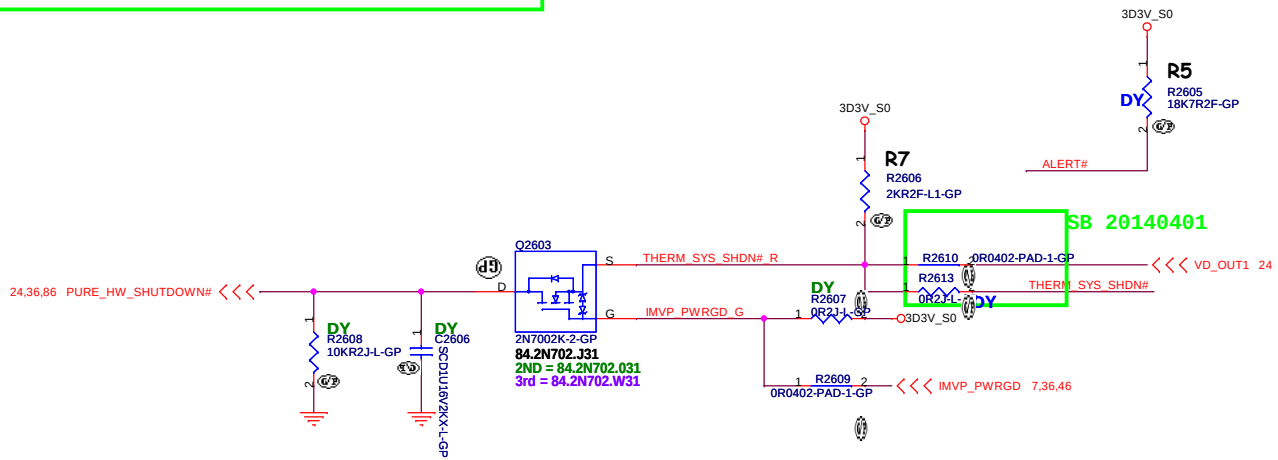
Thermal sensor G788











ALERT# /T_CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

HADES

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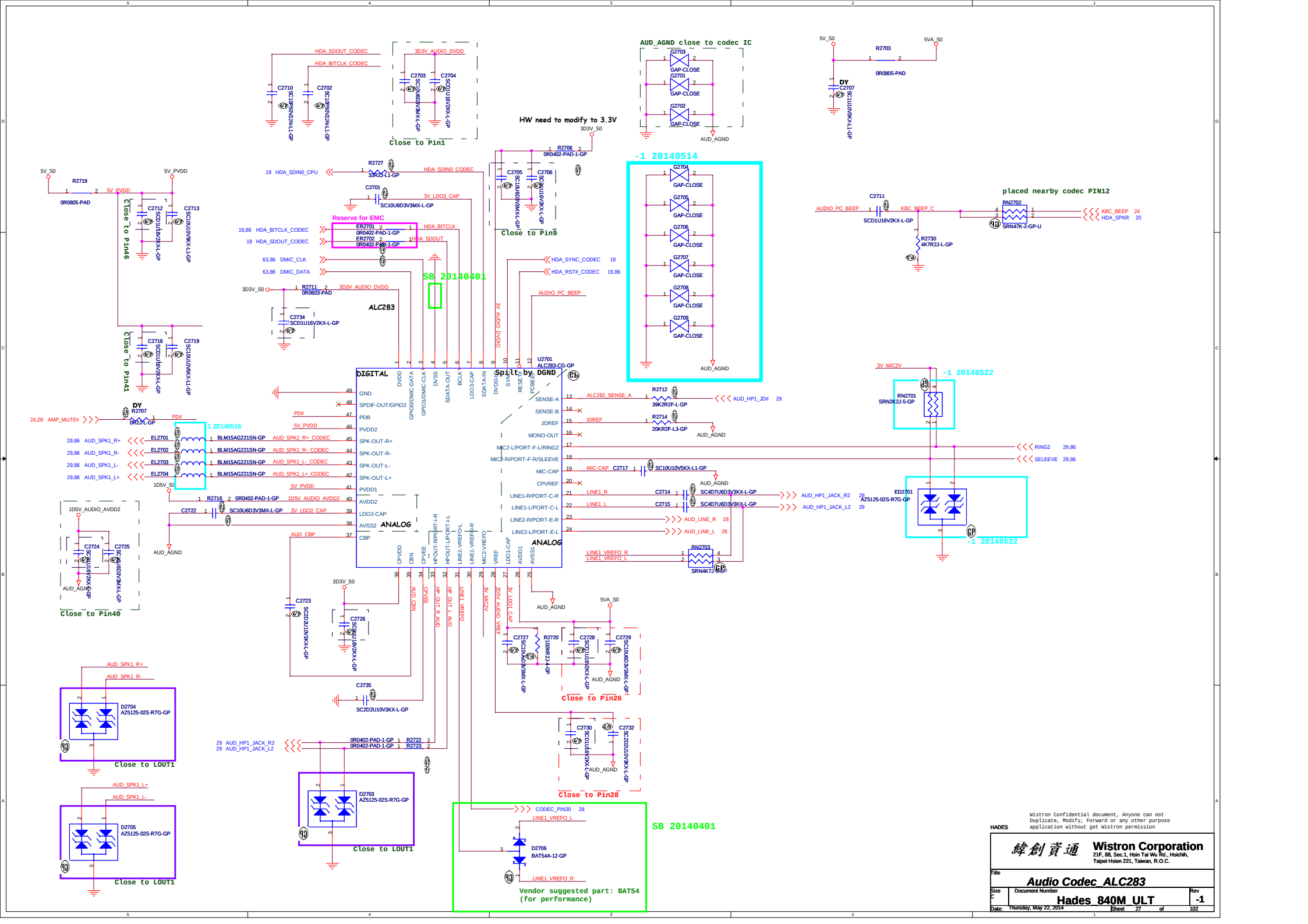
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal 7718/Fan Controllor P2793

Size: A3 | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, May 14, 2014 | Sheet 26 of 102



SB 20140331

-1 20140514

3D3V_S0

R2810
10KR2J-L-GP

D2804
BAS16PT-GP

DY

2ND = 83.00016.K11
3rd = 83.00016.H11

CODEC_PIN30 27

AMP_PD#

D2803
BAW56-5-GP

83.00056.Q11
2nd = 83.00056.R11

AMP_MUTE# 24,27

HDA_RST#_CODEC 19,27

Output Gain Table

R1	R2	R3	R4	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

SB 20140401

5V_S0

R2809
0R0603-PAD

5V_AMP_PVDD

C2801
SC1U10V2KX-L1-GP

C2802
SC10U10V5KX-L1-GP

SB 20140414

SB 20140318

27 AUD_LINE_R

C2805
SC1U10V2KX-L1-GP

AMP_LINE_RC

R2801
1K43R2F-1-GP

R2807
2KR2F-L1-GP

AMP_LINE_RR

C2803
SC1U10V2KX-L1-GP

AMP_RC

SB 20140401

27 AUD_LINE_L

C2806
SC1U10V2KX-L1-GP

AMP_LINE_LC

R2802
1K43R2F-1-GP

R2808
2KR2F-L1-GP

AMP_LINE_LR

C2804
SC1U10V2KX-L1-GP

AMP_LC

AMP_PD#

AMP_BP

C2809
SC2C2ZU10V3KX-L-GP

U2801

PVDD1
PVDD2
INPUT_R
PD#
INPUT_L
BYPASS
GND

OUT_RN
OUT_RP
OUT_LN
OUT_LP
G1
G2

AMP_SPK1_R- 29,86
AMP_SPK1_R+ 29,86
AMP_SPK1_L- 29,86
AMP_SPK1_L+ 29,86

ALC1001-CGT-GP
74.01001.013

Reserve for input attenuation
to have optimized output power

多打ground VIA !!!!!!!!

AMP_SPK1_R+
AMP_SPK1_R-

D2801
AZ5125-02S-R7G-GP

AMP_SPK1_L-
AMP_SPK1_L+

D2802
AZ5125-02S-R7G-GP

5V_S0

R1 DY R2803 0R2J-2-GP

R2 DY R2804 0R2J-2-GP

G1

G2

R3 R2805 0R0402-PAD-1-GP

R4 R2806 0R0402-PAD-1-GP

HADES

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio AMP_ALC1001

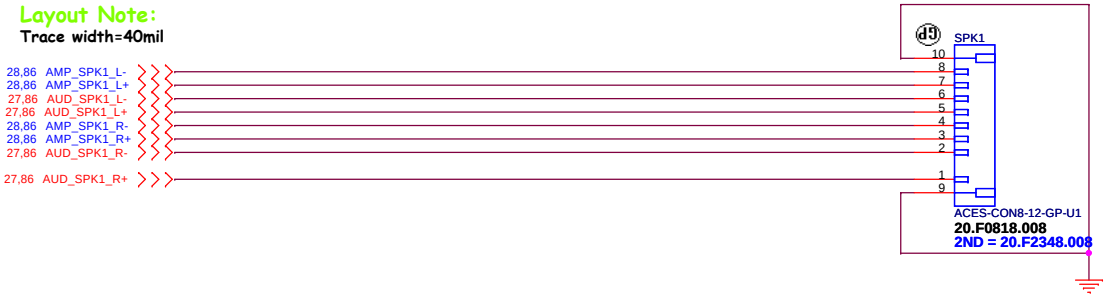
Size: A3 | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, May 14, 2014 | Sheet 28 of 102

SSID = AUDIO

Speaker

Layout Note:
Trace width=40mil

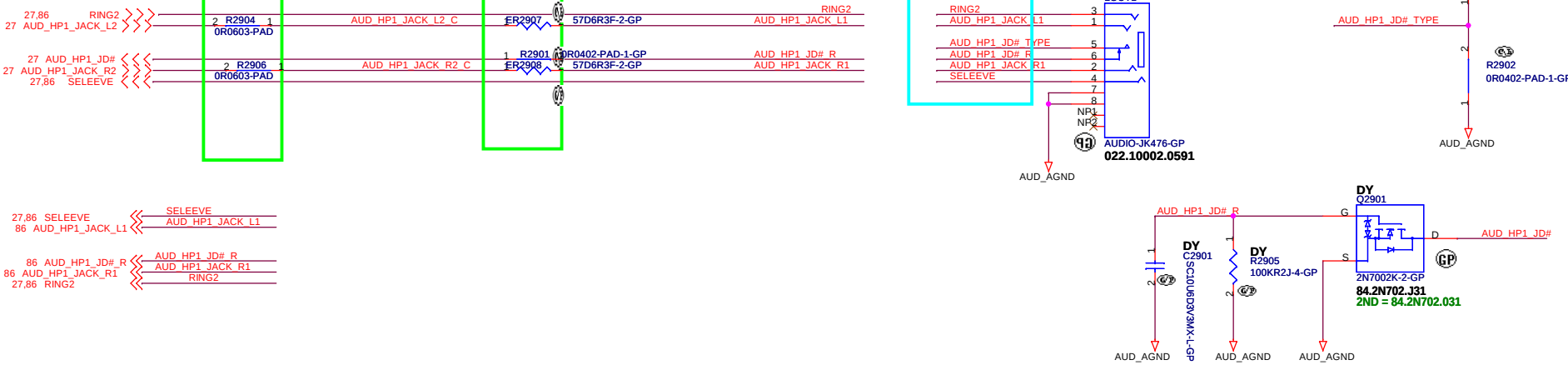


Combo Jack

SB 20140410

SB 20140410

-1 20140522



HADES

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Jack**

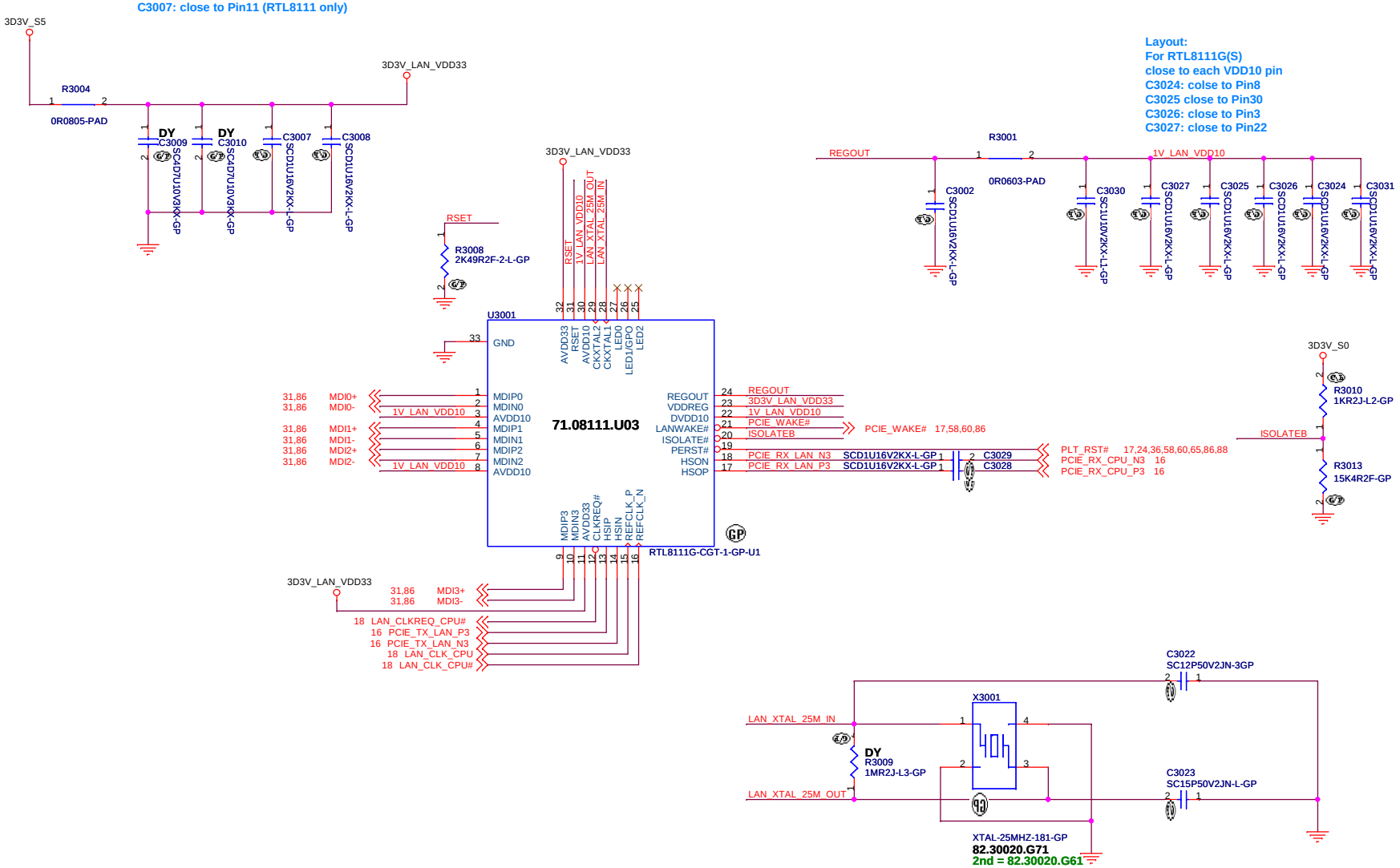
Size	Document Number	Rev
Custom	Hades 840M ULT	-1

Date: Thursday, May 22, 2014 Sheet 29 of 102

40 mils

C3008: close to Pin32
C3007: close to Pin11 (RTL8111 only)

Layout:
For RTL8111G(S)
close to each VDD10 pin
C3024: colse to Pin8
C3025 close to Pin30
C3026: close to Pin3
C3027: close to Pin22



HADES

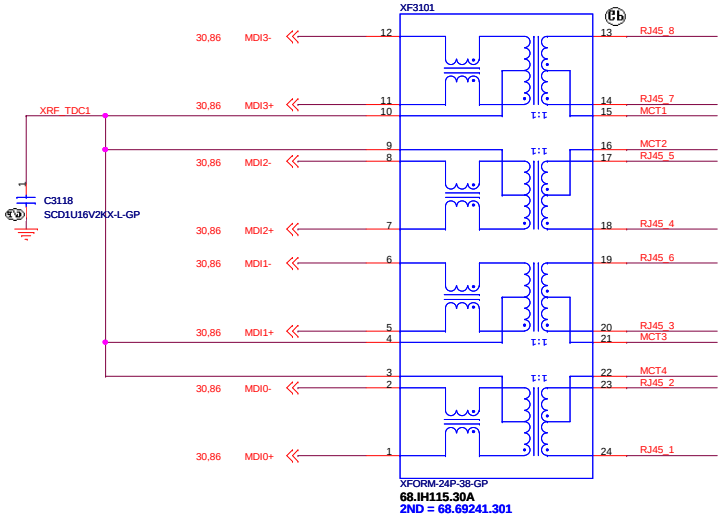
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

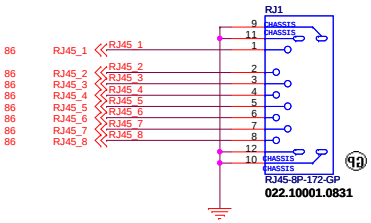
Title: LAN (RTL8111G(S))

Size	Document Number	Rev
A3	Hades_840M_ULT	-1

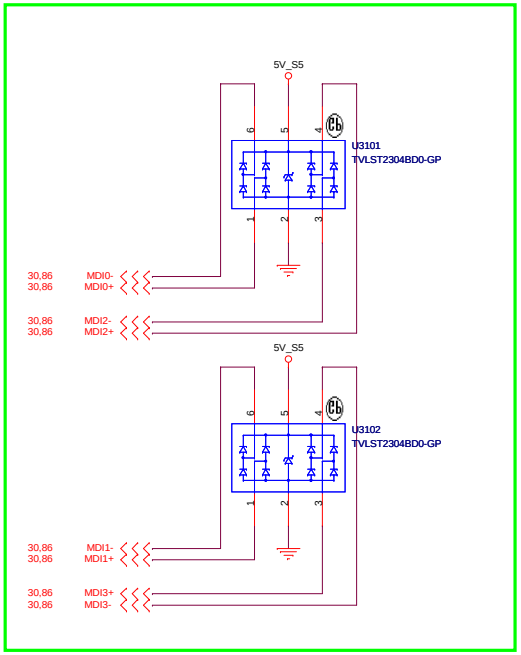
Date: Wednesday, April 30, 2014 Sheet 30 of 102

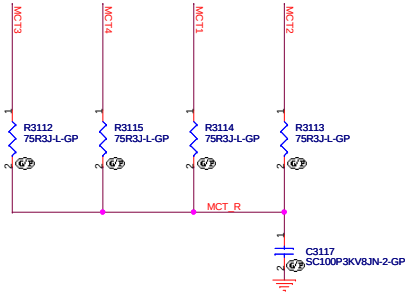
SSID = LAN





SB 20140328 FOR POE ISSUE





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Title: *(LAN+VGA) CONNECTOR*

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 31 of 102

HADES

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Title

RTS5170(CARD READER)

Size	Document Number	Rev
A4	Hades_840M_ULT	-1
Date: Wednesday, April 30, 2014	Sheet 32 of 102	

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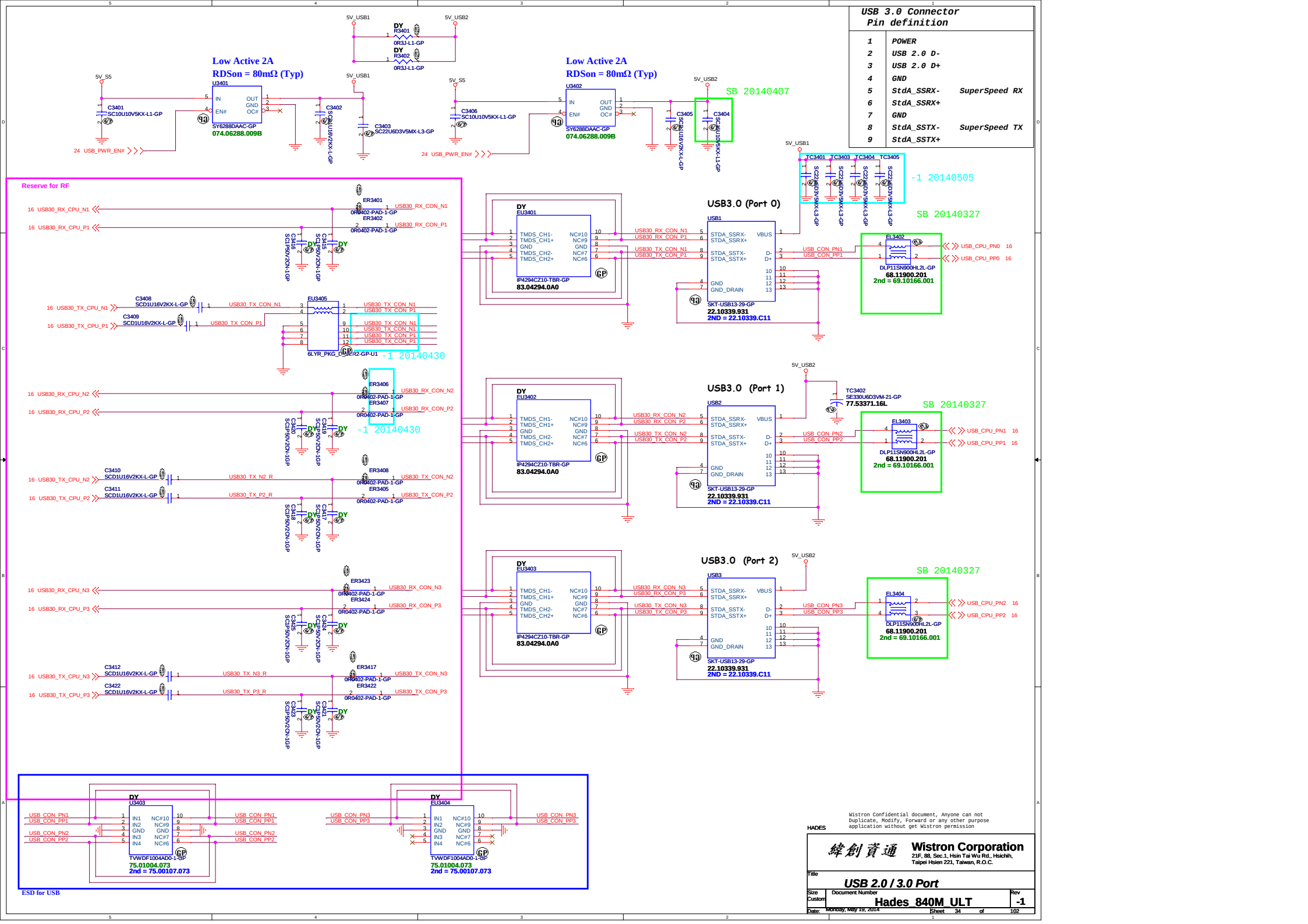
Title

Card Reader CONN (Reserved)

Size	Document Number	Rev
Custom	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 33 of 102


USB 3.0 Connector Pin definition
1 POWER
2 USB 2.0 D-
3 USB 2.0 D+
4 GND
5 StdA_SSRX- SuperSpeed RX
6 StdA_SSRX+
7 GND
8 StdA_SSTX- SuperSpeed TX
9 StdA_SSTX+
Low Active 2A
RDSon = 80mΩ (Typ)
SY6288DAAC-GP
074.06288.009B
SB 20140407
Reserve for RF
USB3.0 (Port 0)
USB3.0 (Port 1)
USB3.0 (Port 2)
IP4294CZ10-TBR-GP
83.04294.0A0
SKT-USB13-29-GP
22.10339.931
2ND = 22.10339.C11
DLP11SN900HL2L-GP
68.11900.201
2nd = 69.10166.001
TVWDF1004AD0-1-GP
75.01004.073
2nd = 75.00107.073
ESD for USB
-1 20140505
SB 20140327
-1 20140430
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Title
USB 2.0 / 3.0 Port
Size Custom
Document Number
Hades_840M_ULT
Rev -1
Date: Monday, May 19, 2014
Sheet 34 of 102

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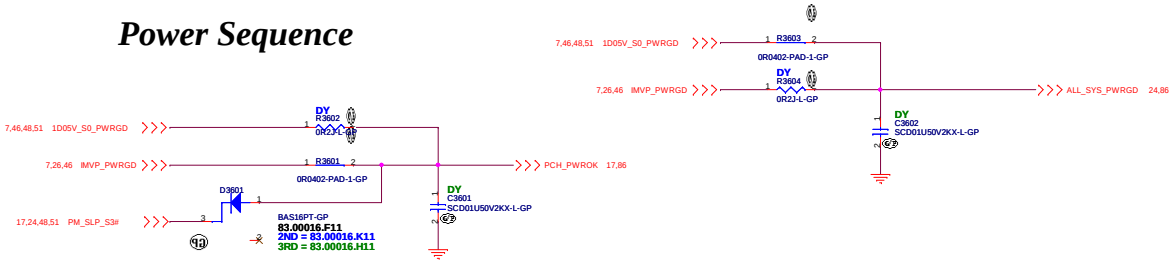
Title

USB CHARGER

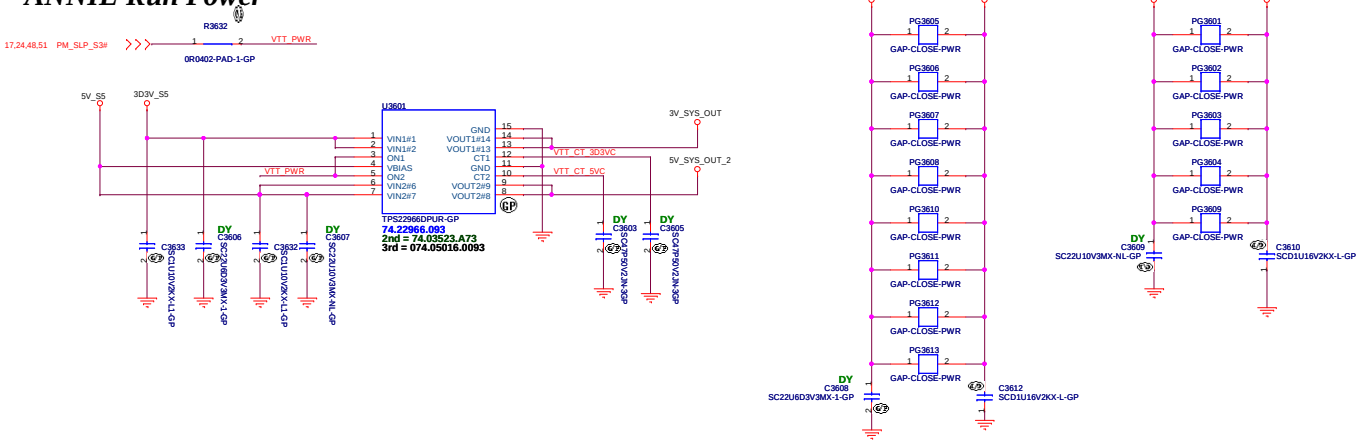
Size	Document Number	Rev
A4	**Hades 840M ULT**	**-1**

Date: Wednesday, April 30, 2014 Sheet 35 of 102

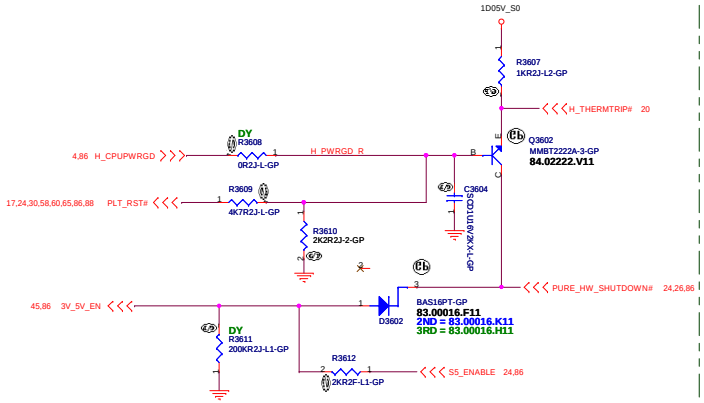
Power Sequence

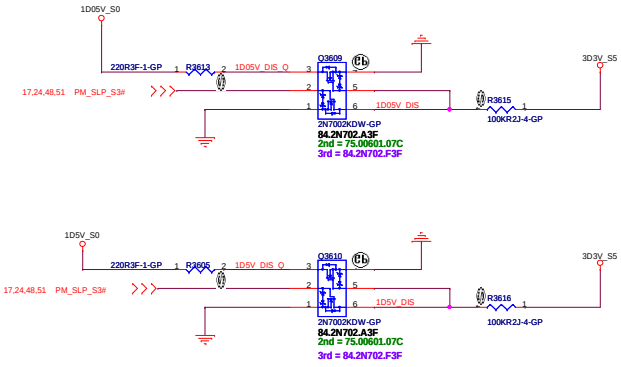


ANNIE Run Power



Discharge circuit





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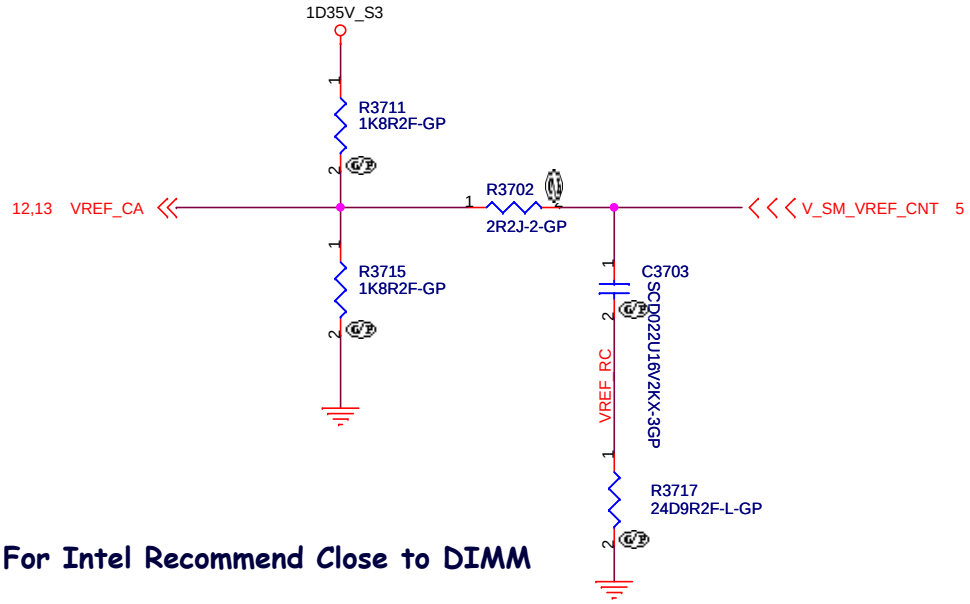
Title: Power Plane Enable & SEQUENCE

Size: A2 | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, May 14, 2014 | Sheet 38 of 102



For Intel Recommend Close to DIMM

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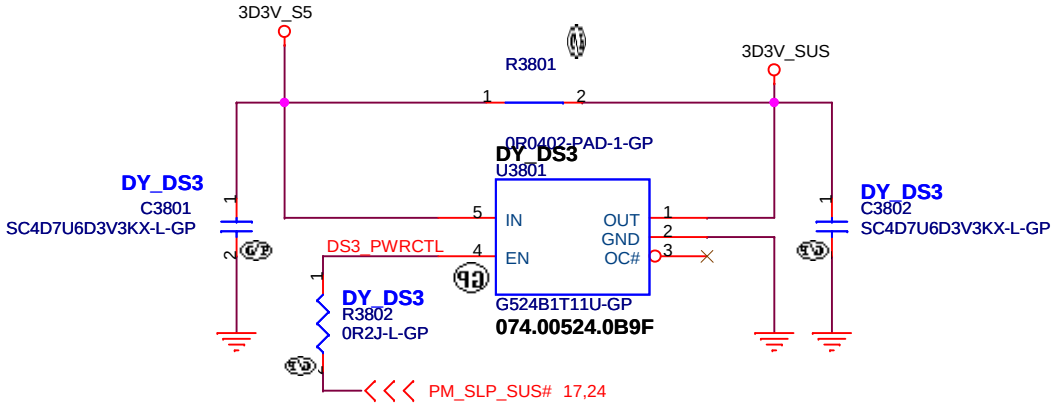
Title: ADAPTER OCP / S3 reduction

Size	Document Number	Rev
Custom	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 37 of 102



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Title: ***DS3***

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

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Title

1D05_M

Size	Document Number	Rev
A4	**Hades_840M_ULT**	-1

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Title

Connected Standby1

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

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Title

Connected Standby2

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

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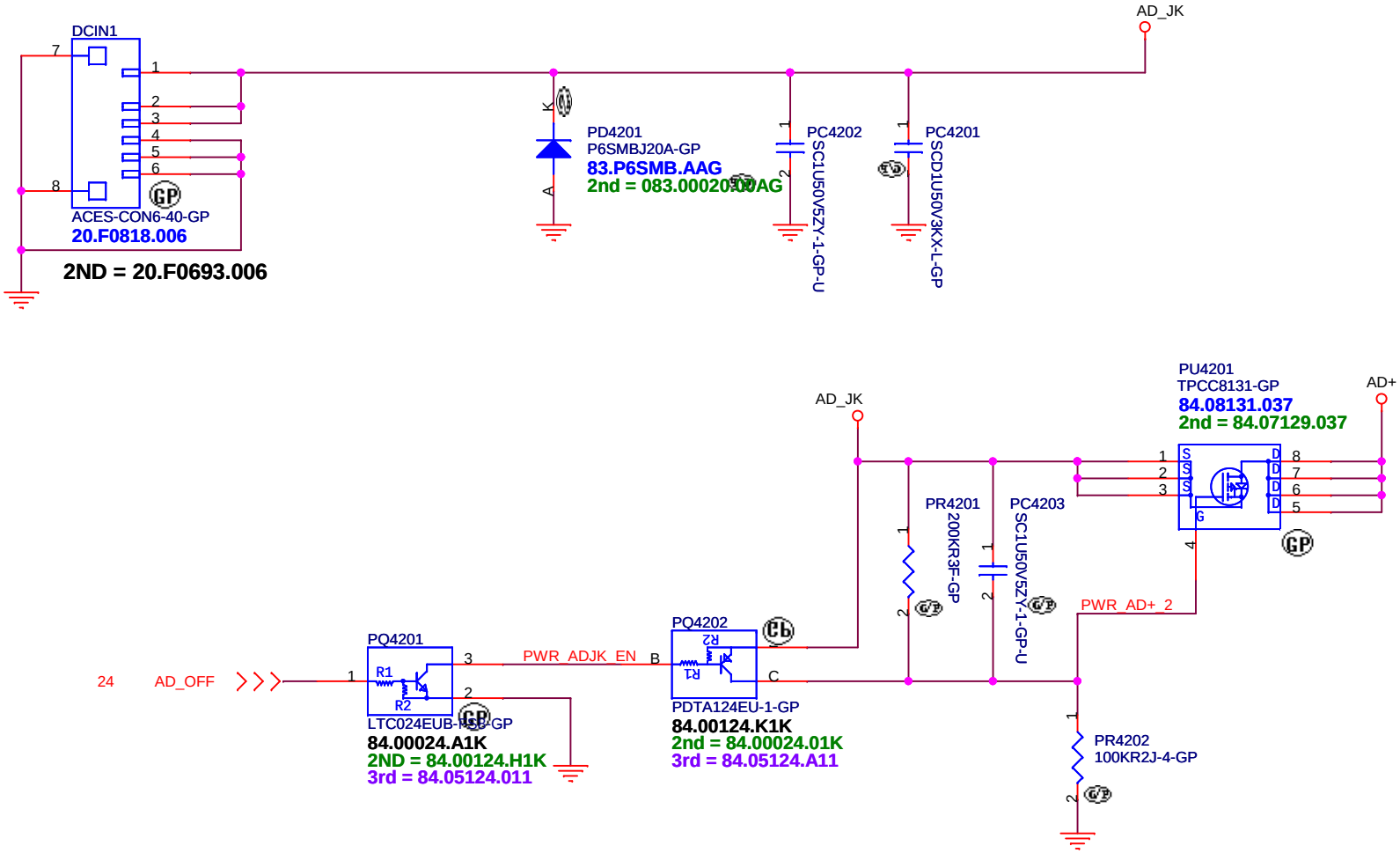
ANNIE solution

Adaptor in to generate DCBATOUT



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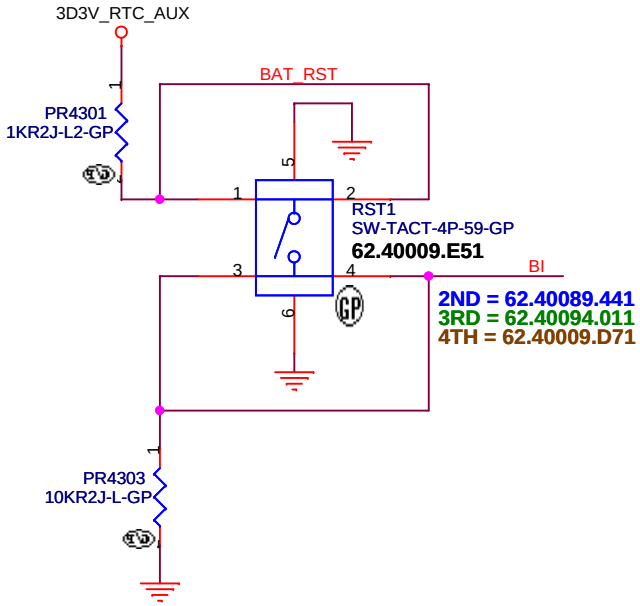
Title: **DCIN JACK**

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Friday, May 16, 2014 Sheet 42 of 102

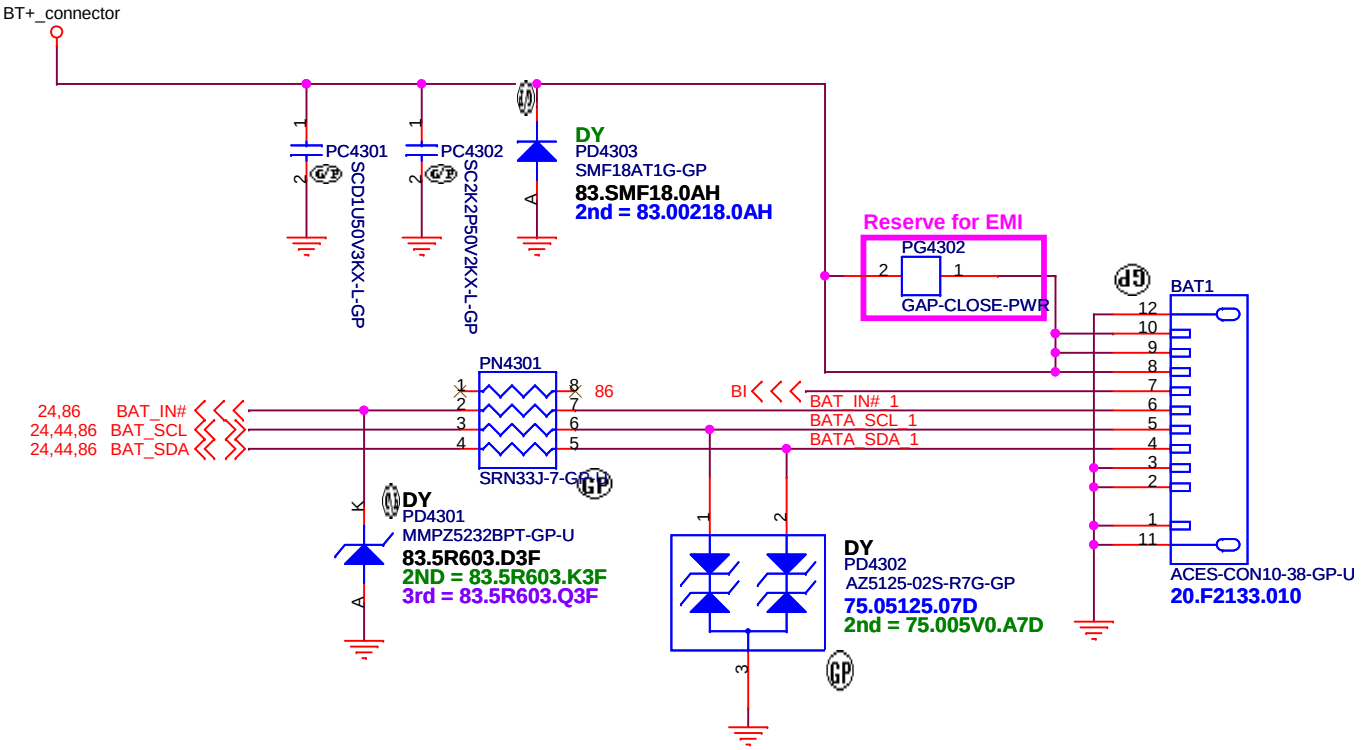
Battery Reset



SB 20140401

Battery Insert

Battery Connector



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Title: ***BATT CONN***

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

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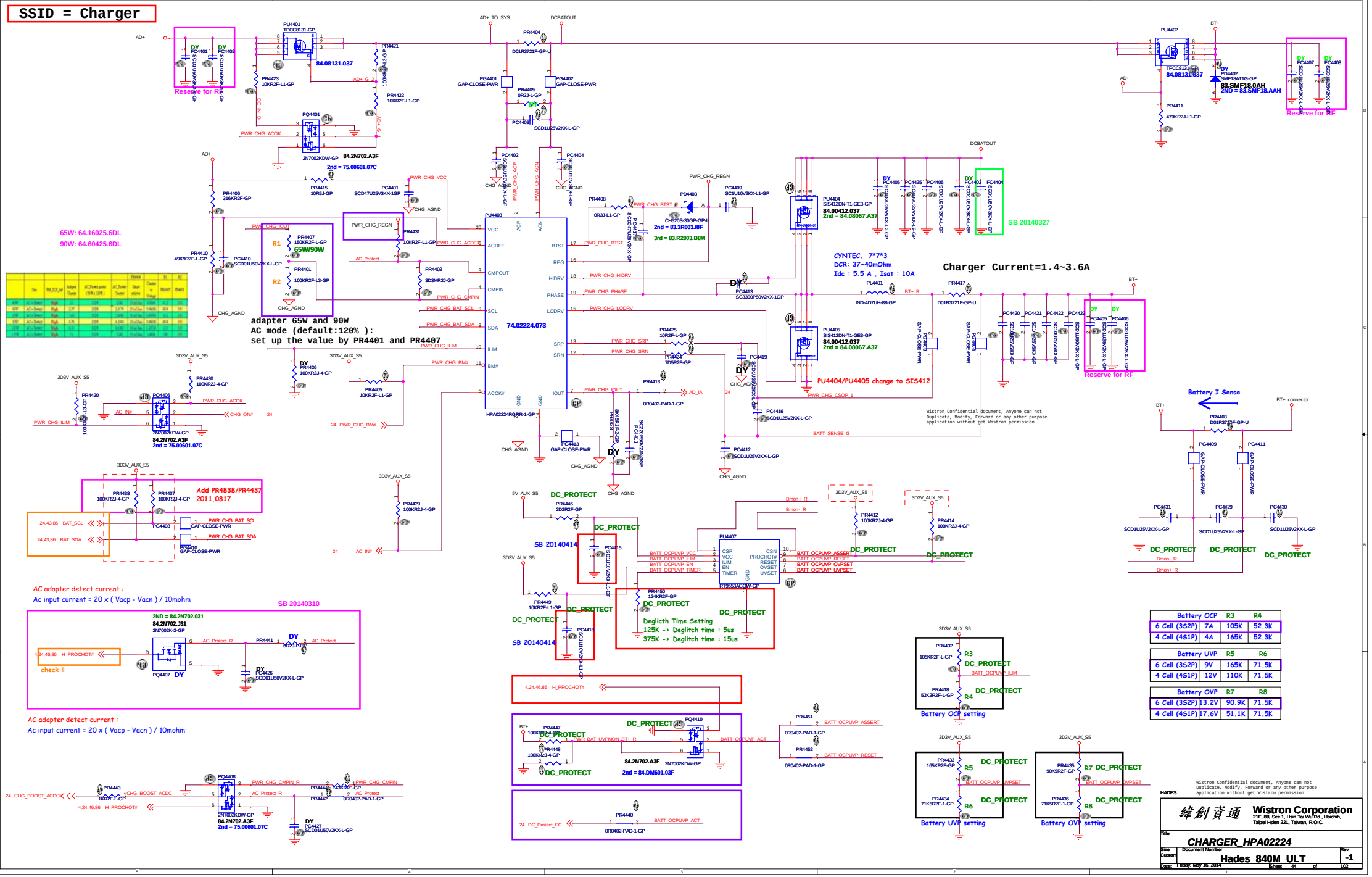
SSID = Charger



Battery OCP	R3	R4
6 Cell (3S2P)	7A	105K	52.3K
4 Cell (4S1P)	4A	165K	52.3K

Battery UVP	R5	R6
6 Cell (3S2P)	9V	165K	71.5K
4 Cell (4S1P)	12V	110K	71.5K

Battery OVP	R7	R8
6 Cell (3S2P)	13.2V	90.9K	71.5K
4 Cell (4S1P)	17.6V	51.1K	71.5K

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Title: CHARGER_HPA02224

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

Date: Friday, May 16, 2014 | Sheet 44 of 102

SSID = PWR.Plane.Regulator_3p3v5v

SB 20140401

SB 20140401

High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Choke
MagLayers. 7x7x3 , 2R2
Dcr : 18 ~ 20 mOhm
Idc : 8A Isat : 14 A

High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Choke
MagLayers. 7x7x3 , 2R2
Dcr : 18 ~ 20 mOhm
Idc : 8A Isat : 14 A

Iomax=4.306A
(3.476+0.83)
OCP>6A

Design Current = 5.925A
3.625+2.3
9A<OCP

74.51225.B73

Close outcap

220uF/6.3V, 6.3*6*4.5
ESR=17mohm
Ripple Current=3200 mA

Close outcap

220uF/6.3V, 6.3*6*4.5
ESR=17mohm
Ripple Current=3200 mA

net PWR_5V_VOUT1 , use 20mil

SB 20140403

EA40-HW SB

Close to VFB Pin (pin5)

Vout = 2 * (1 + R1/R2)
= 2 * (1 + 6.8K / 10K)
= 3.36V

Close to VFB Pin (pin2)

Vout = 2 * (1 + R1/R2)
= 2 * (1 +33K / 21K)
= 5.14V

20140122

3D3V OCP setting

5V OCP setting

Reserve for RF

Reserve for RF

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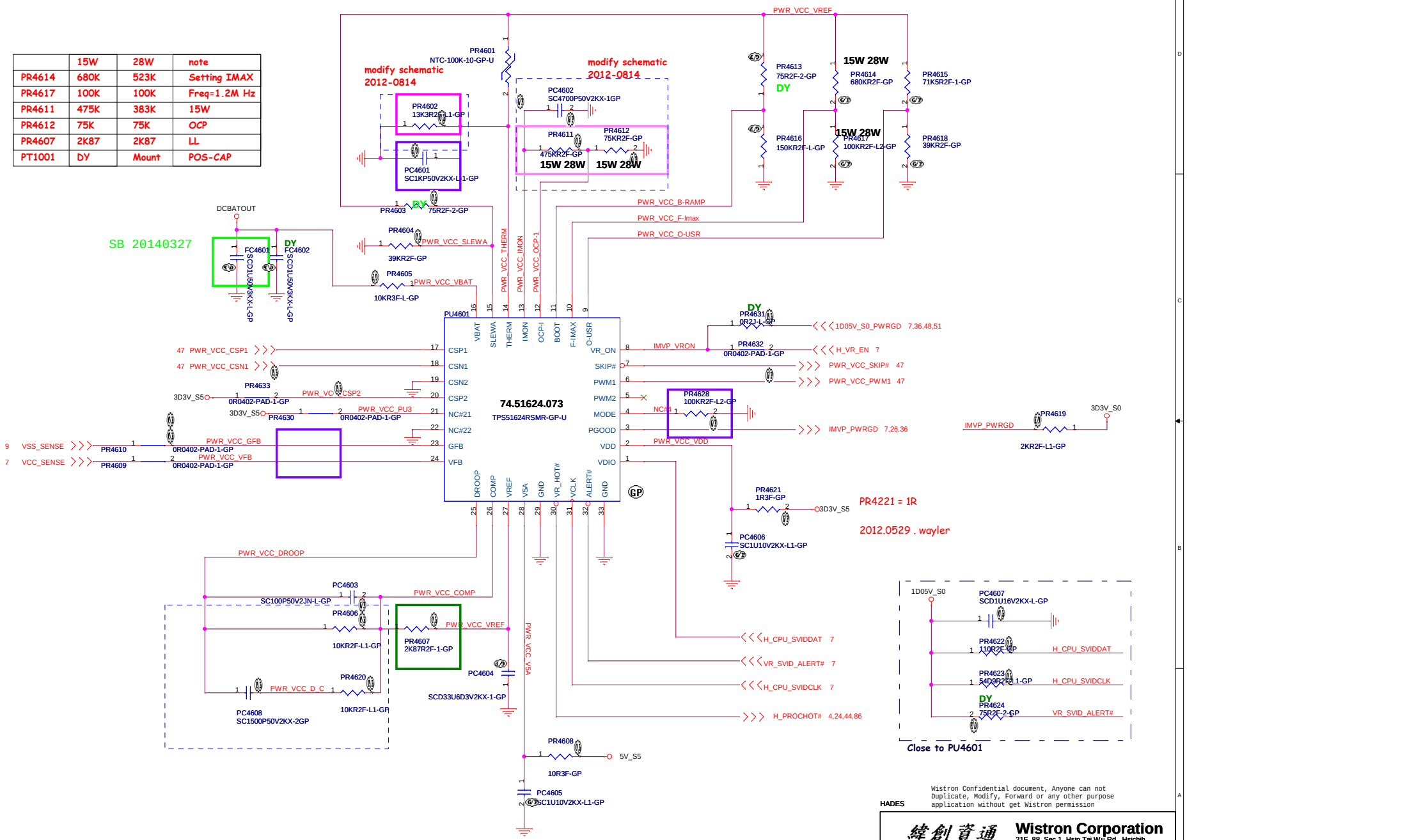
Title: TPS51225_5V/3D3V

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 45 of 102

SSID = CPU.Regulator

	15W	28W	note
PR4614	680K	523K	Setting IMAX
PR4617	100K	100K	Freq=1.2M Hz
PR4611	475K	383K	15W
PR4612	75K	75K	OCP
PR4607	2K87	2K87	LL
PT1001	DY	Mount	POS-CAP



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Title: ***TPS51624_CPUCORE(1/2)***

Size	Document Number	Rev
Custom	Hades_840M_ULT	-1

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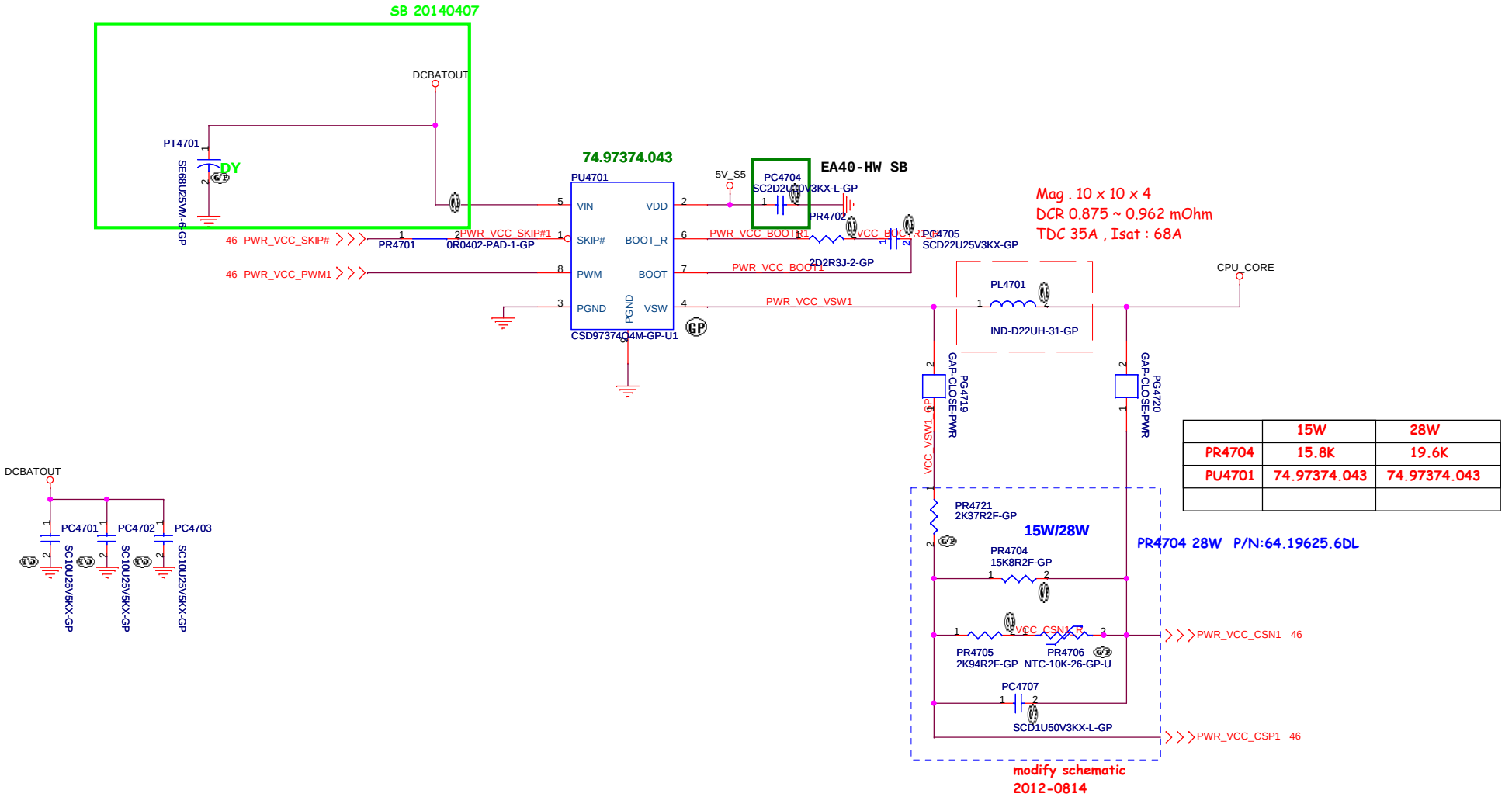

	15W	28W
PR4704	15.8K	19.6K
PU4701	74.97374.043	74.97374.043

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Title: TPS51624_CPUCORE(2/2)

Size: B | Document Number: Hades_840M_ULT | Rev: -1

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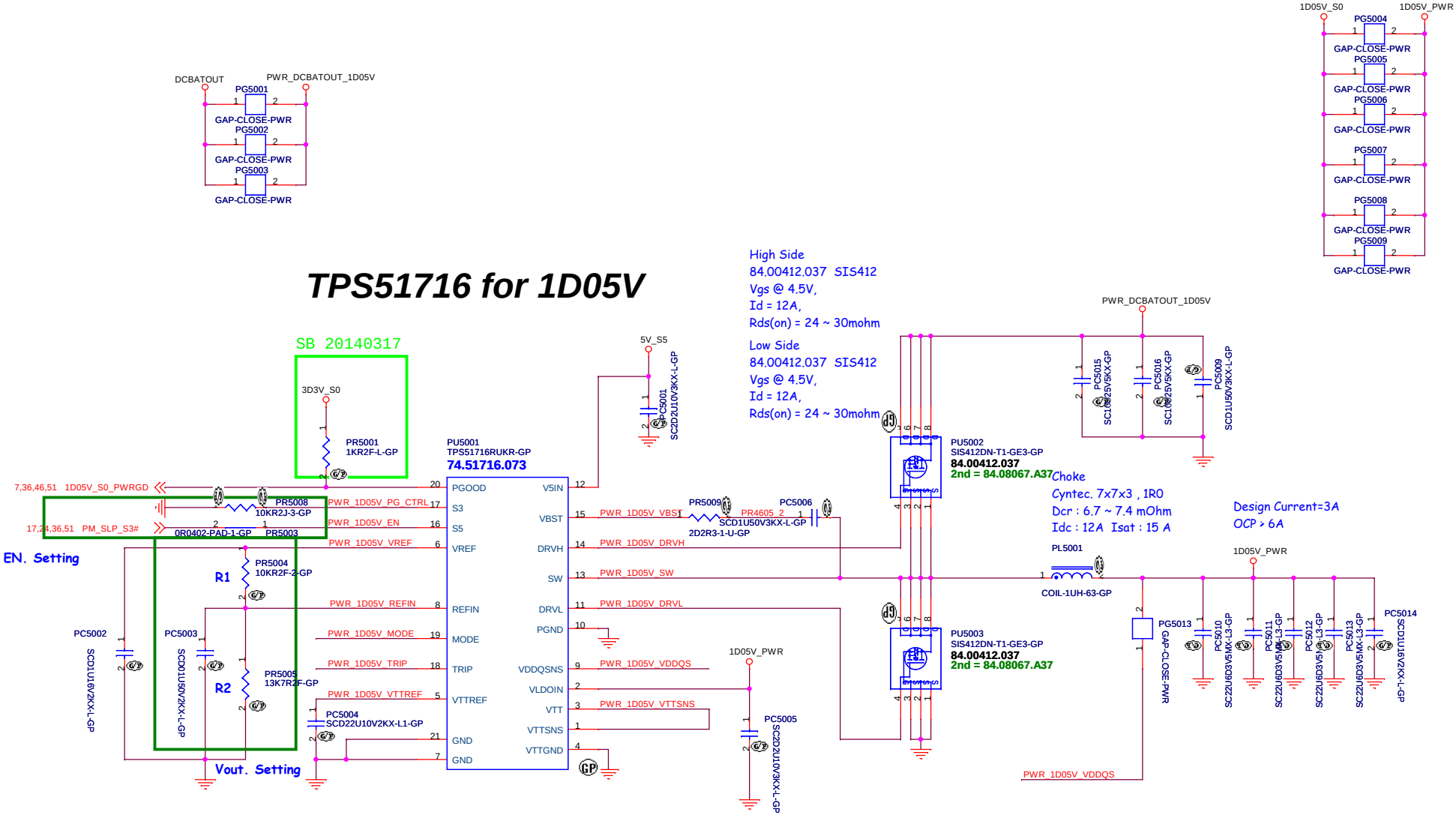
TPS51716 for 1D05V



MODE

PR5006	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

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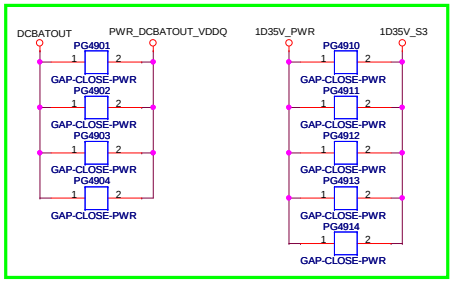
Title: DC to DC_1D05V(SY8208D)

Size: A3 | Document Number: Hades_840M_ULT | Rev: -1

Date: Friday, May 16, 2014 | Sheet 48 of 102

SSID = PWR.Plane.Regulator_1p2v0p6v

RT8231 for VDDQ



SB 20140328

High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

OCP setting

Close to pin23

Close to pin23

SB 20140328

Iomax=1A
OCP>1.5A

PU4901 change to RT8207M

Close to output cap pin1, not inside of the output cap

Vout=0.675 x (1+R1/R2)
=0.675 x (1+20/20)
=1.35

Close to PIN9

Choke
Cyntec. 7x7x3 , 1R0
Dcr : 6.7 ~ 7.4 mOhm
Idc : 12A Isat : 15 A

IccMAX = 4.4A
OCP > 8A

EA40-HW 1

+0.675VS
Iomax: 1.2A

SB 20140328

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Title: RT8231(VDDQ_VTT)

Size: Custom | Document Number: Hades_840M_ULT | Rev: -1

Date: Wednesday, April 30, 2014 | Sheet 49 of 102

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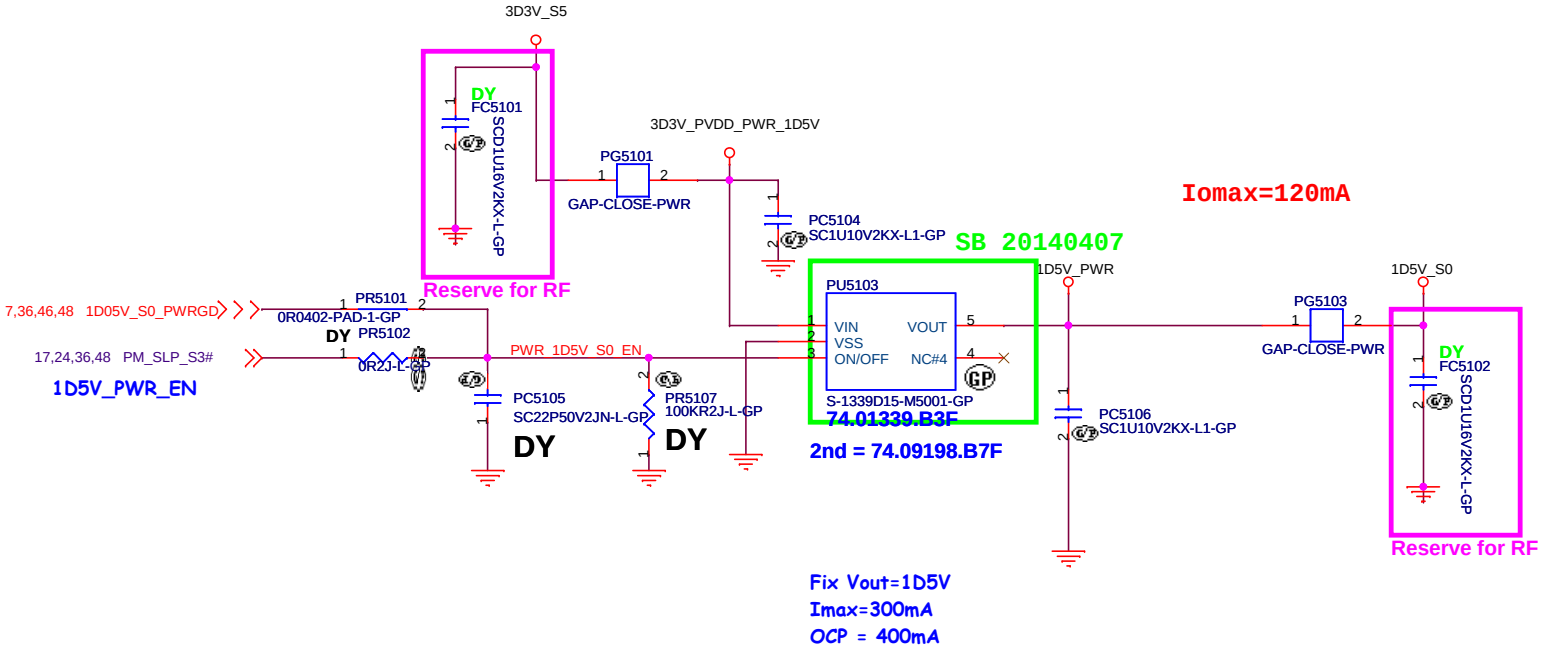
Title

1D8V_S0 TLV62065

Size	Document Number	Rev
A4	Hades_840M_ULT	-1
Date: Wednesday, April 30, 2014	Sheet 50 of 102	

TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V



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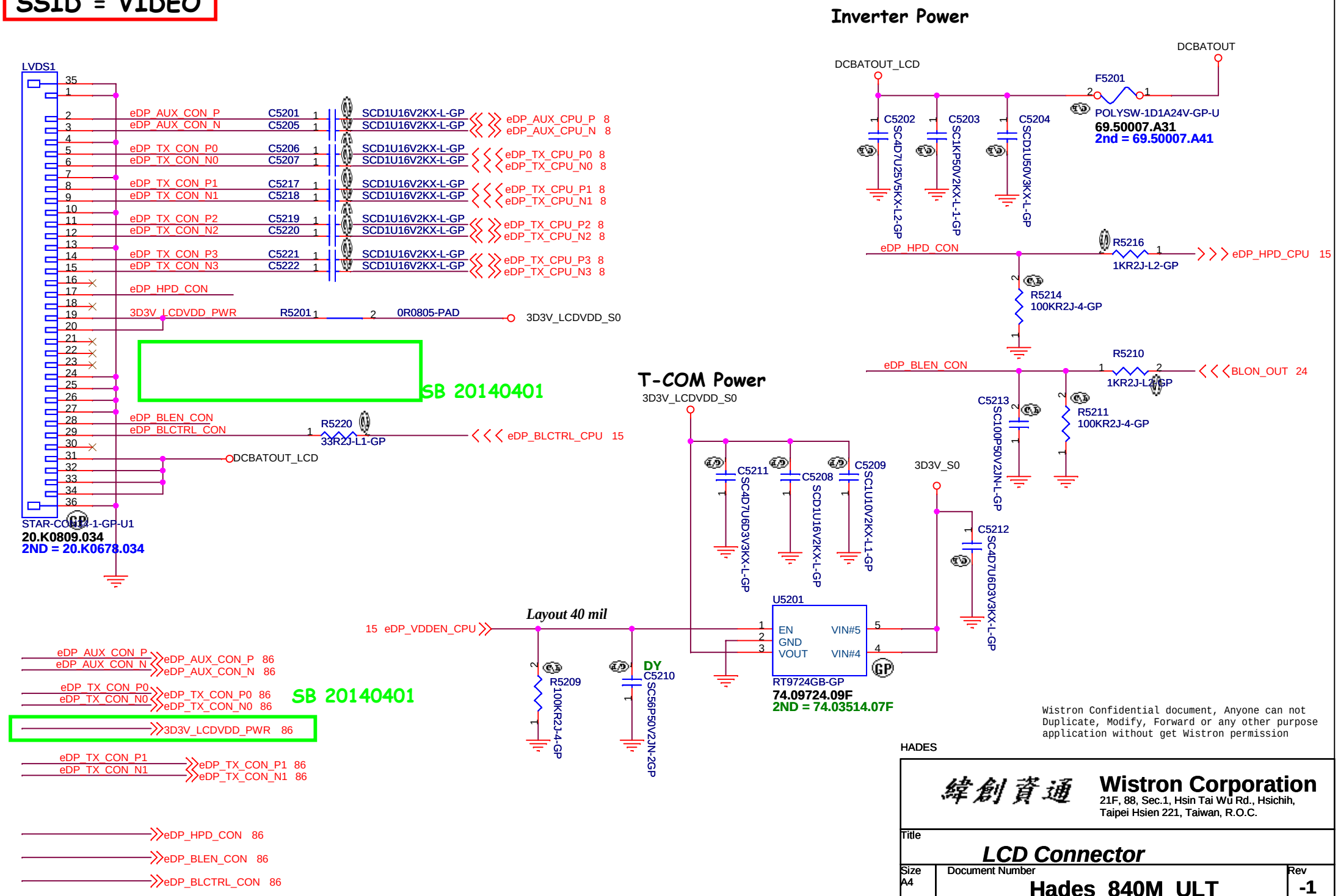
Title: *1D5V_S0 SYW232*

Size	Document Number	Rev
Custom	Hades_840M_ULT	-1

Date: Thursday, May 15, 2014 Sheet 51 of 102

SSID = VIDEO



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Title: LCD Connector

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 52 of 102

HADES

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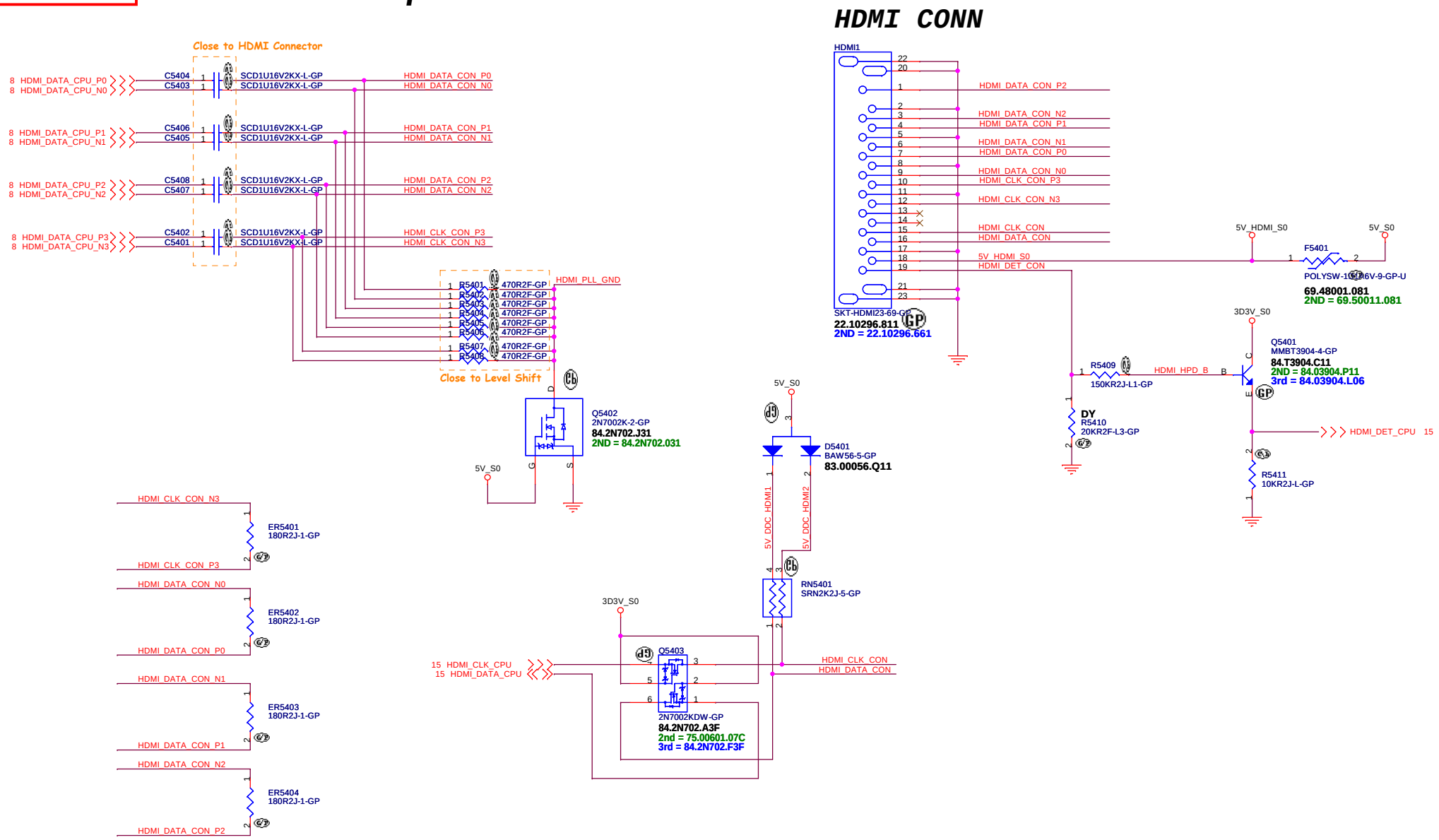
Title

CRT Board Connector (Reserved)

Size	Document Number	Rev
A4	Hades_840M_ULT	-1
Date: Wednesday, April 30, 2014	Sheet 53 of 102	

SSID = VIDEO

HDMI Level Shifter & CONNECTOR



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Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
A3	Hades_840M_ULT	-1

Date: Friday, May 09, 2014 Sheet 54 of 102

HADES

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Title

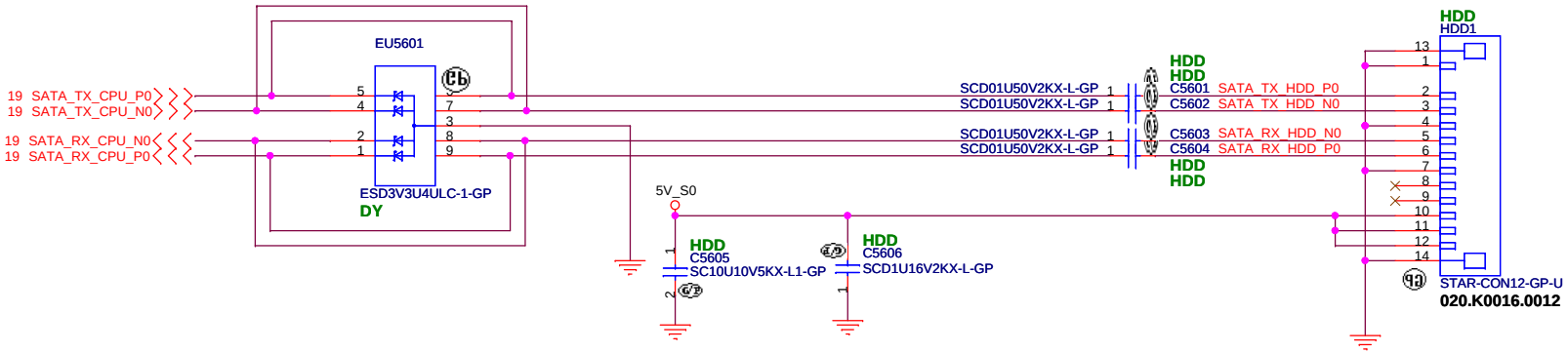
Display Port

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 55 of 102

SSID = SATA

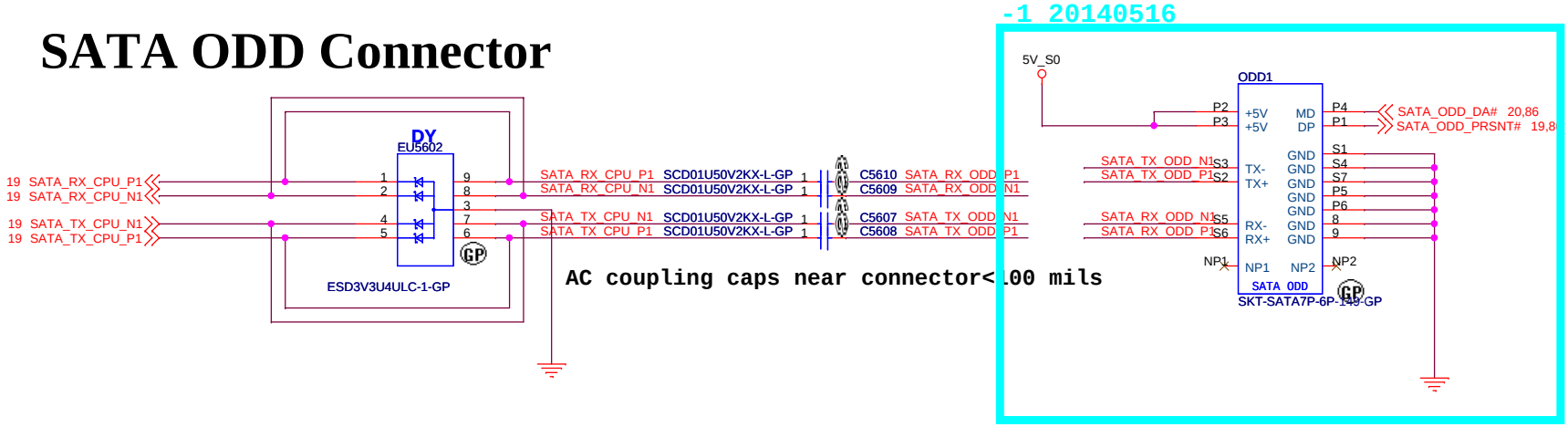
SATA HDD Connector



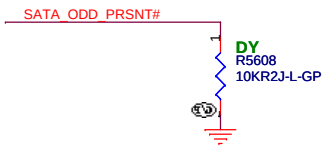
AC coupling caps near connector<100 mils

SATA ODD Connector

-1 20140516



AC coupling caps near connector<100 mils



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Title: ***HDD / ODD***

Size	Document Number	Rev
Custom	Hades_840M_ULT	-1

Date: Friday, May 16, 2014 Sheet 56 of 102

HADES

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Title

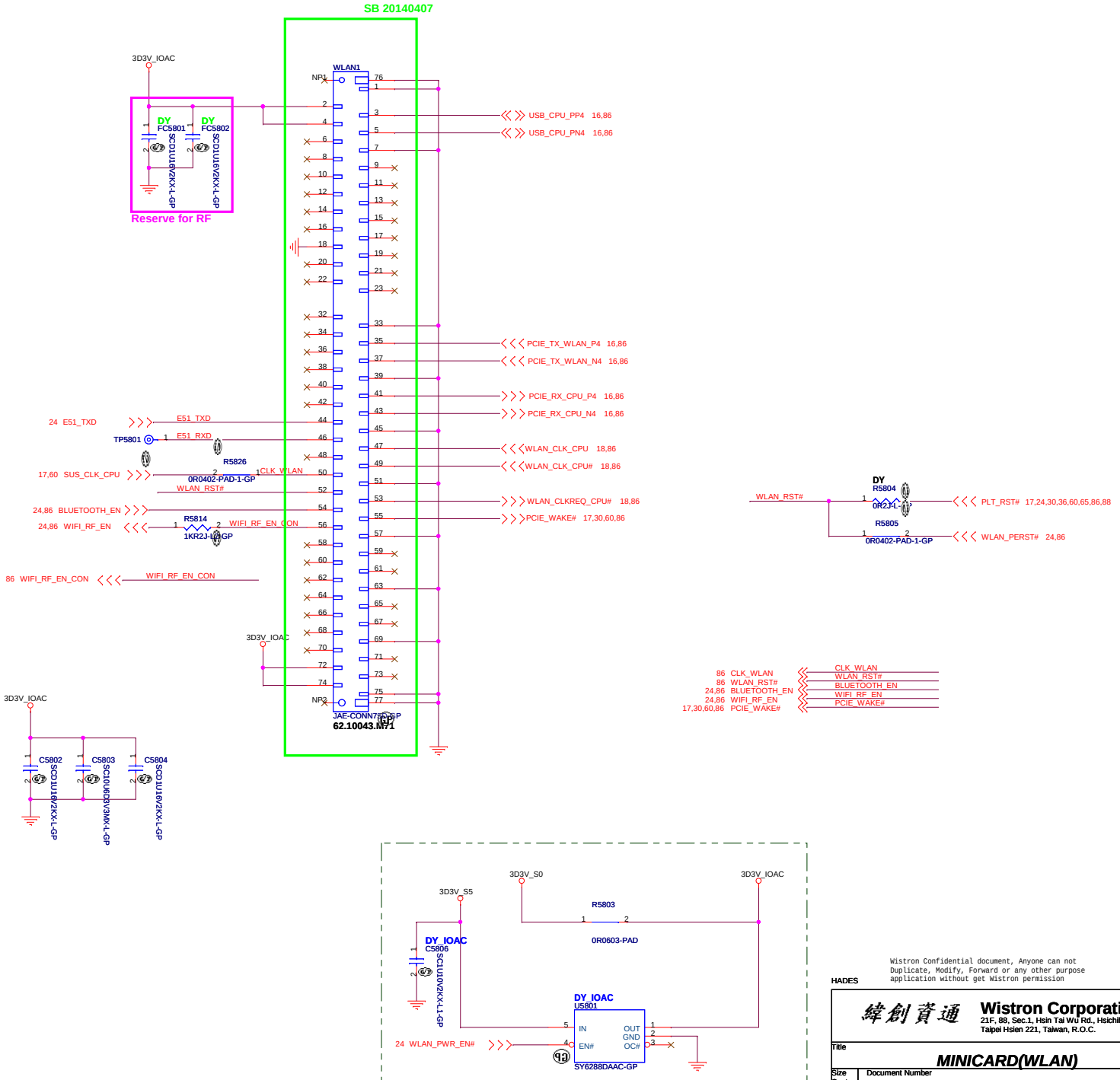
E-SATA

Size	Document Number	Rev
A4	Hades_840M_ULT	-1

Date: Wednesday, April 30, 2014 Sheet 57 of 102

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



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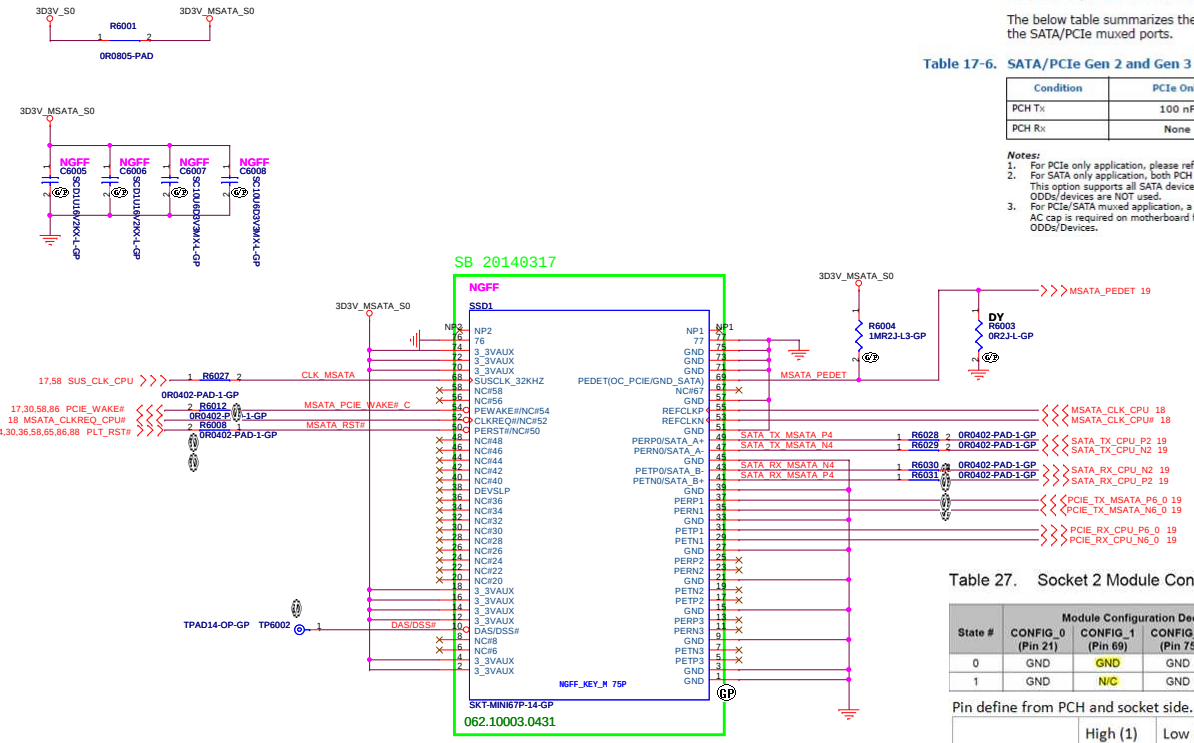
SSID = m-SATA

Mini Card Connector (NGFF m-SATA)



17.2.6 General Guidelines for mSATA (Gen 2 and Gen 3) Routing on SATA/PCIe muxed Ports

The below table summarizes the AC cap requirements on the motherboard when using the SATA/PCIe muxed ports.

Table 17-6. SATA/PCIe Gen 2 and Gen 3 Capacitor Values

Condition	PCIe Only	SATA Only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF[2]	None[3]

Notes:
1. For PCIe only application, please refer to the PCIe guidelines for details.
2. For SATA only application, both PCH Tx and PCH Rx channels need to have 10 nF caps on the motherboard. This option supports all SATA devices. However, the PCH Rx 10 nF capacitor can be removed if DC coupled ODDs/devices are NOT used.
3. For PCIe/SATA muxed application, a 100 nF AC cap is required on motherboards for PCH Tx channel and NO AC cap is required on motherboard for the PCH Rx channel. This option DOES NOT support DC coupled ODDs/Devices.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

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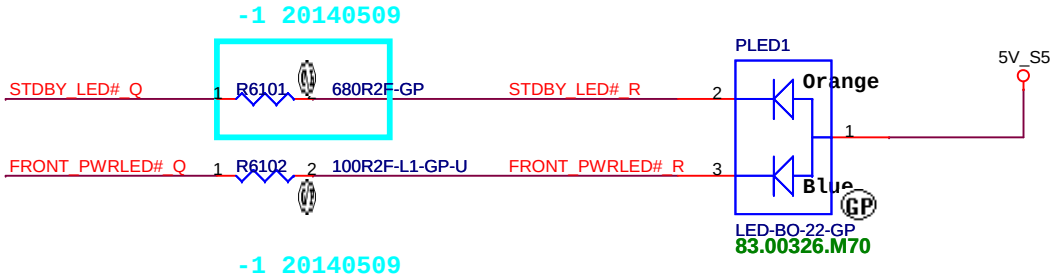
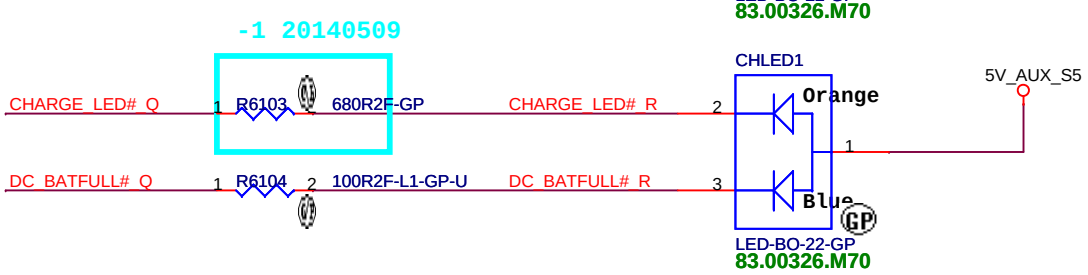
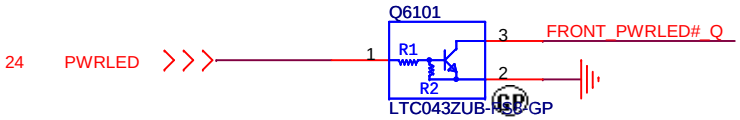
SSID = User.Interface

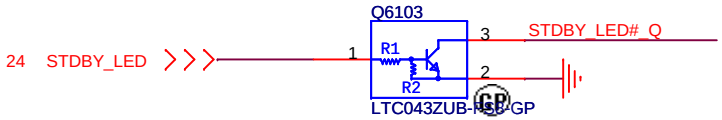




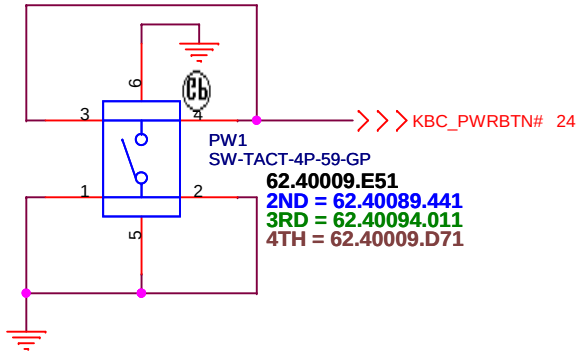
Power Button_LED



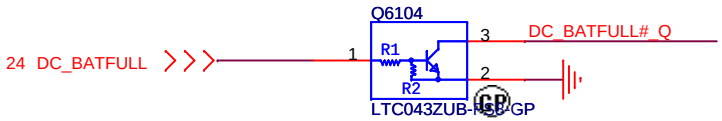
Power STDBY_LED



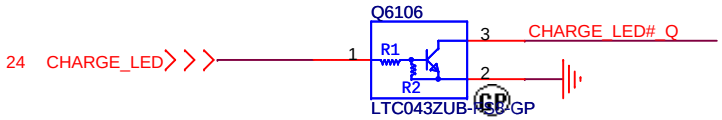
Power Button



Battery LED2(DC_BATFULL)



Battery LED1(CHARGE)



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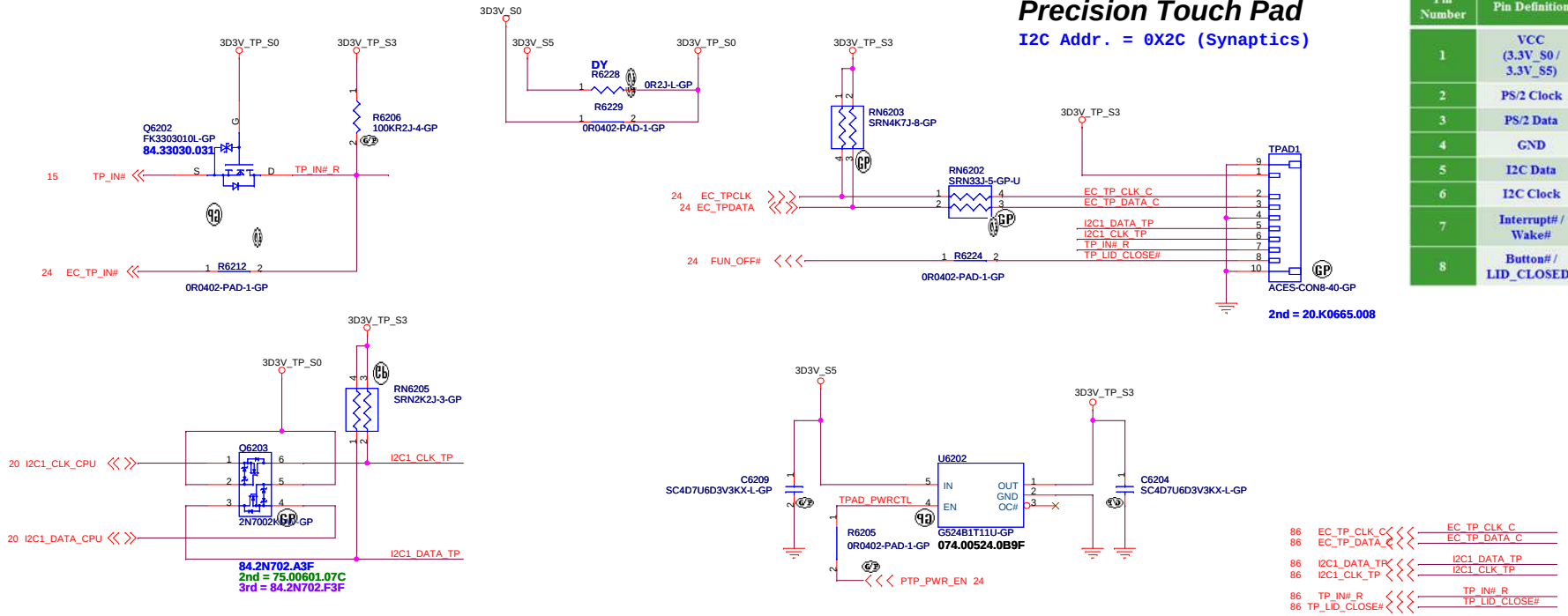
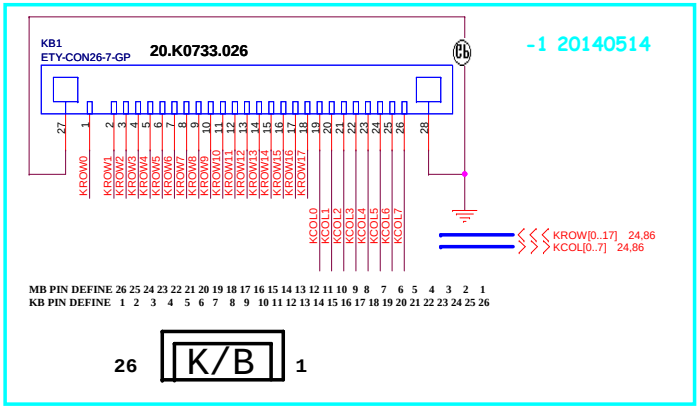
Precision Touch Pad

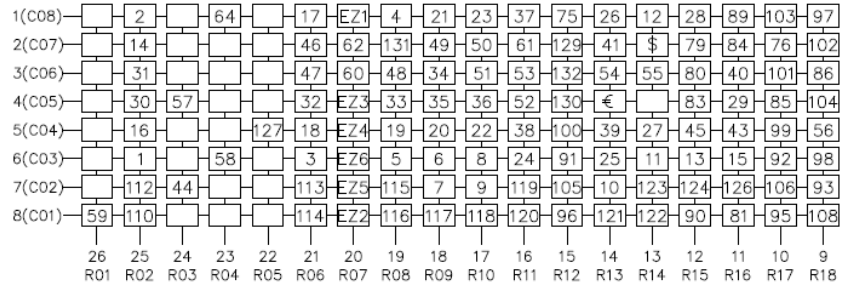
I2C Addr. = 0X2C (Synaptics)

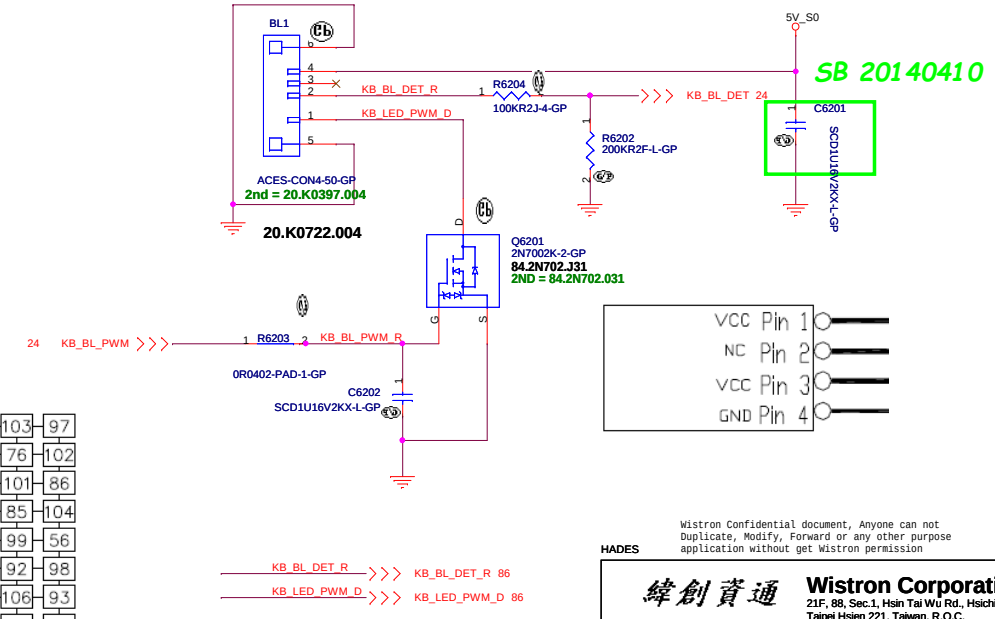
Pin Number	Pin Definition
1	VCC (3.3V_S0 / 3.3V_S5)
2	PS/2 Clock
3	PS/2 Data
4	GND
5	I2C Data
6	I2C Clock
7	Interrupt# / Wake#
8	Button# / LID_CLOSED#



Internal KeyBoard Connector







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Title: **Key Board/Touch Pad**

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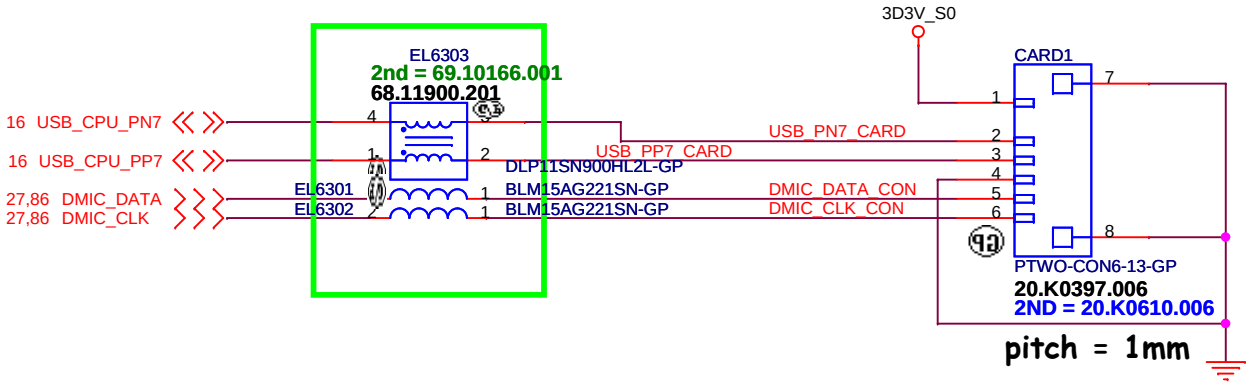
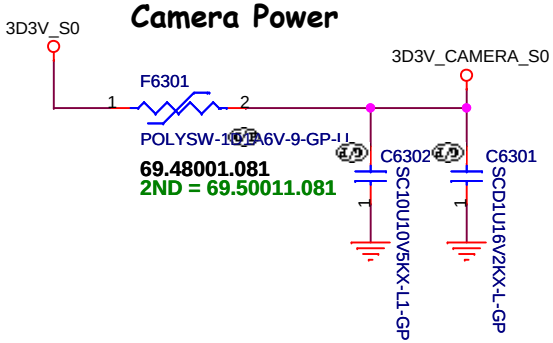
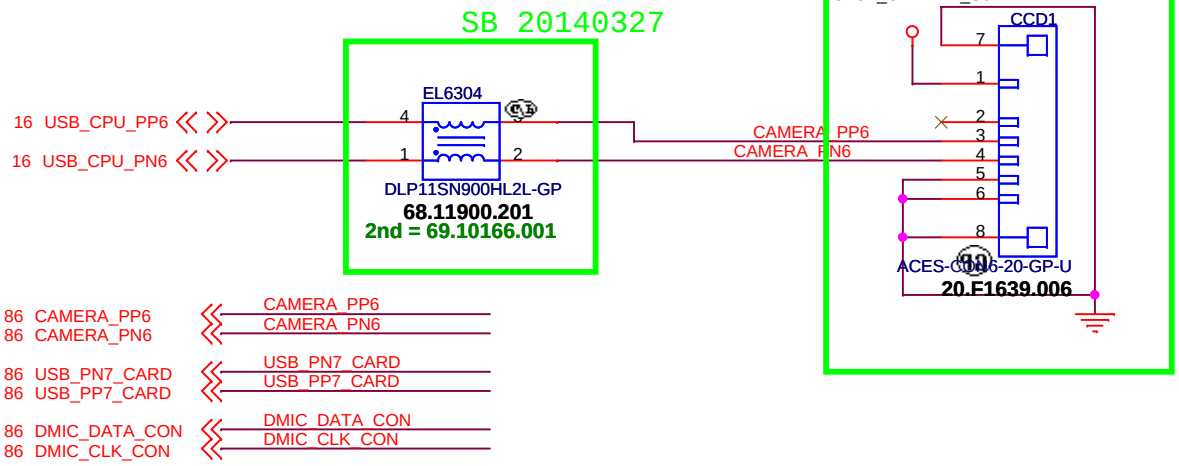
SB 20140327





SB 20140328

SB 20140327



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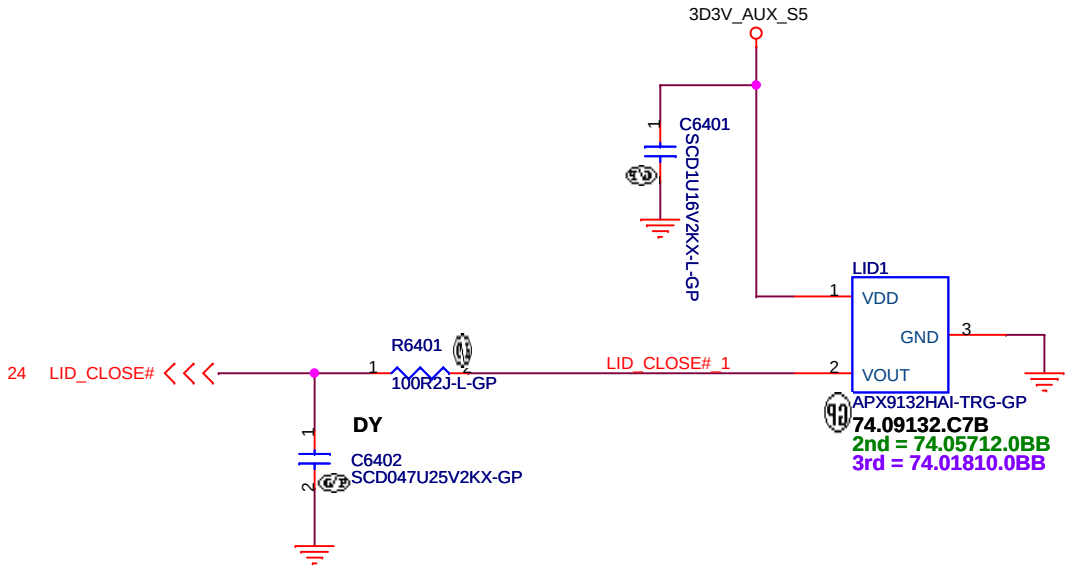

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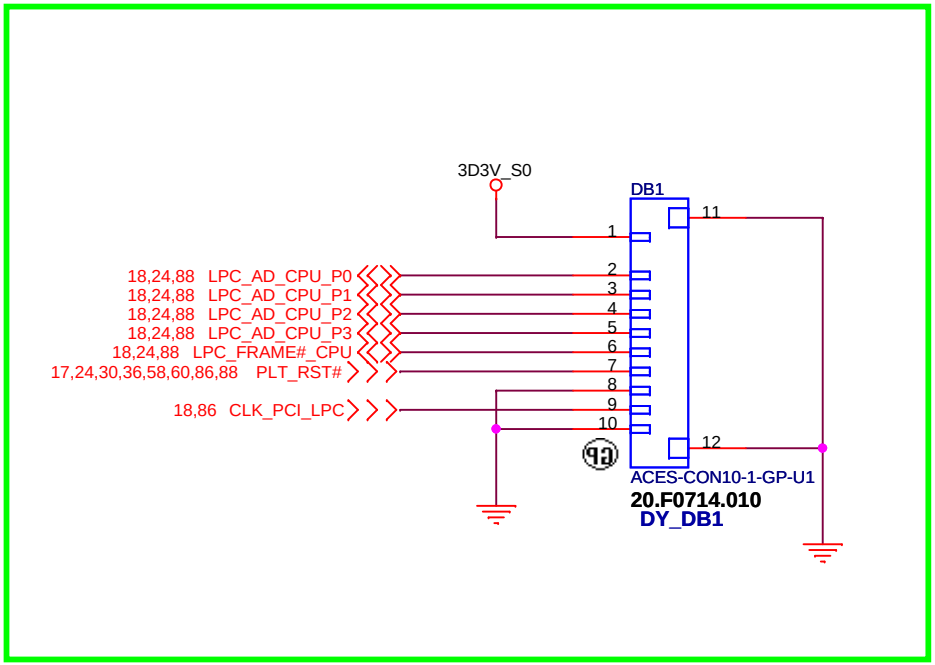
SB 20140401



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Title: ***Dubug connector***

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Title

SENSOR HUB

Size	Document Number	Rev
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G Sensor

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Thunderbolt (1/5)

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Thunderbolt (2/5)

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Thunderbolt (3/5)

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Thunderbolt (4/5)

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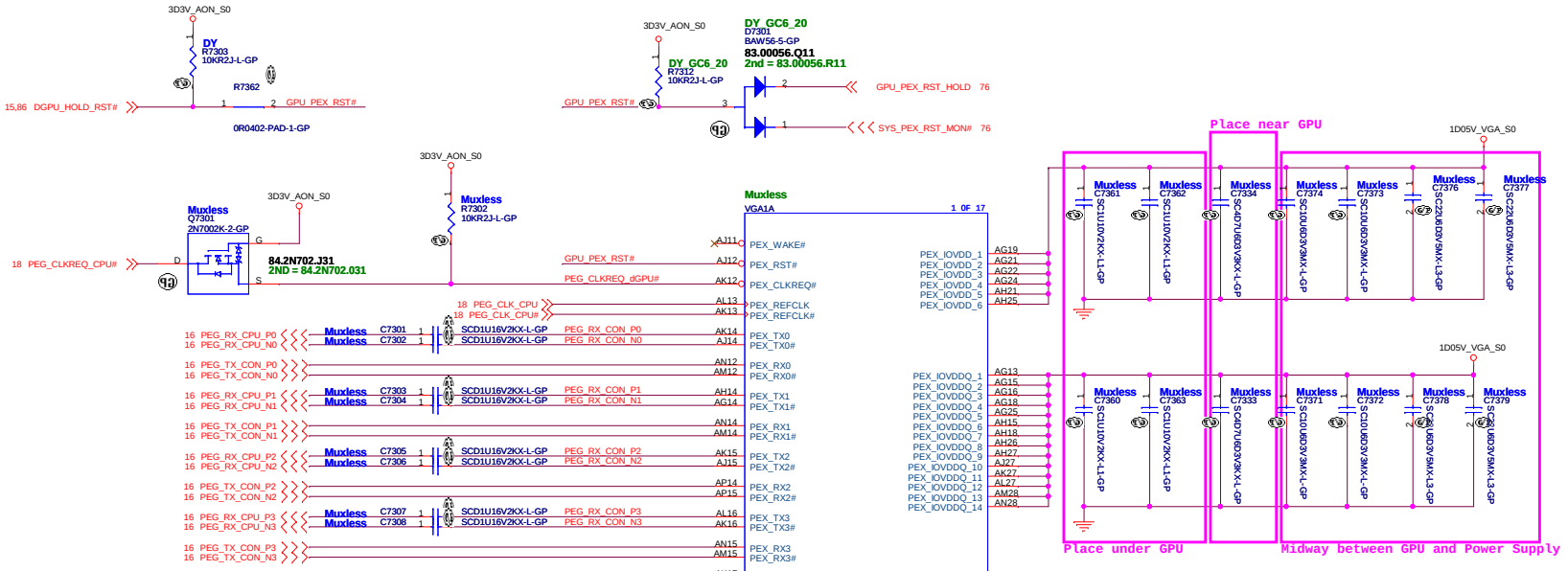

3.4.2 PCI Express Power Decoupling and Filtering

Table 3-16. PEX_IOVVD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply
GB4B-128 GB3-256	1.0 µF	X6S	0402	4	Under GPU
	4.7 µF	X6S	0603	2	Near GPU
	10 µF	X5R	0805	4	Midway between GPU and Power Supply
	22 µF	X5R	0805	4	Midway between GPU and Power Supply

Table 3-18. PEX_SVDD_3V3 and PEX_PLL_HVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 µF	X5R	0402	1	Near GPU
4.7 µF	X5R	0603	2	Near GPU

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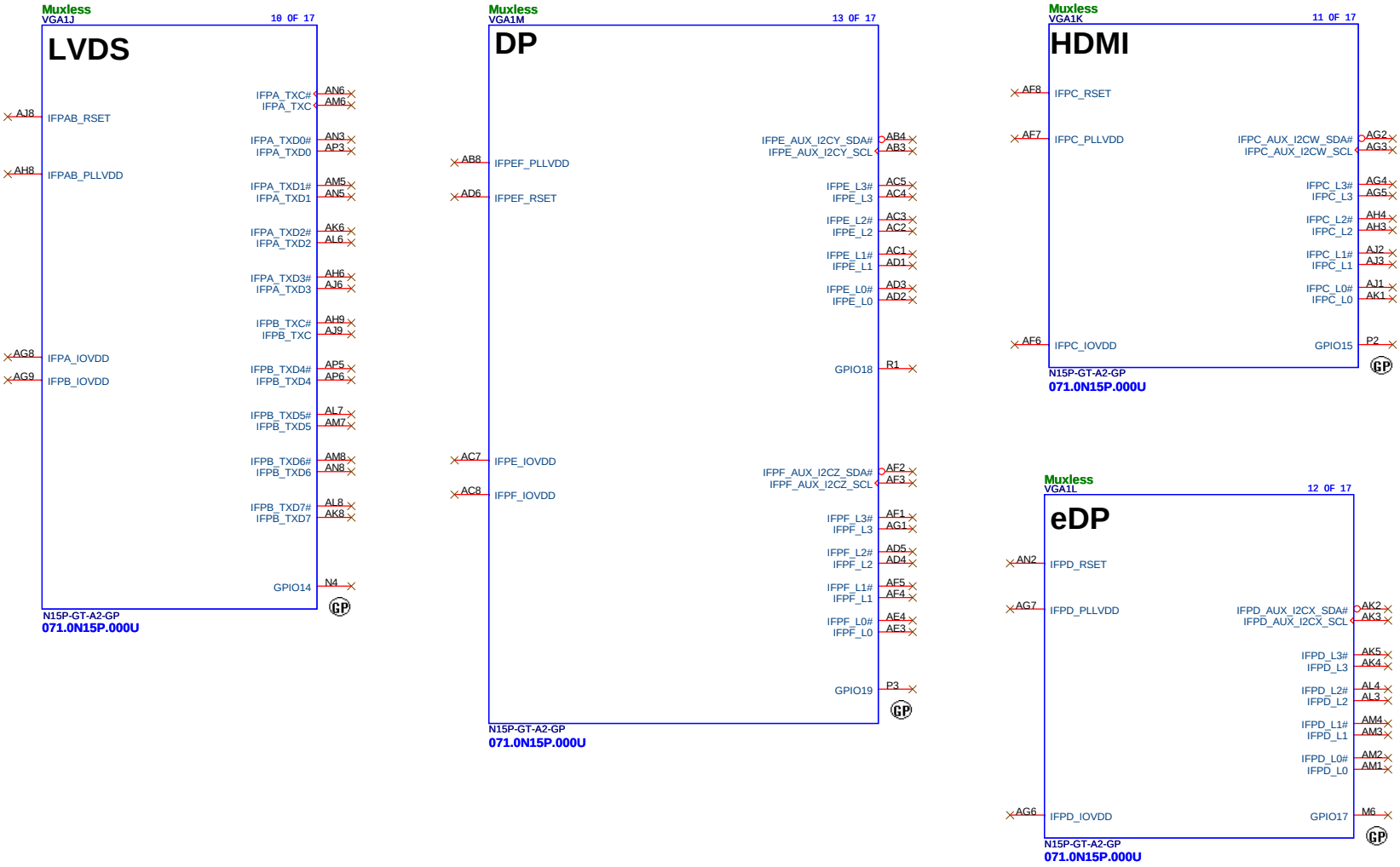

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Mode D Command Mapping
(DG-06803-001_V04_P.76_Table 21)

N15x DDR3 mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#
FBx_CMD31		

FBCLK Termination place on VRAM side

FBCLK Termination place on VRAM side

Group A

Group B

Table 3-10. GDDR5 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type	Footprint	Population		Location
GB2B-64 GDDR5	0.1 µF	X7R	0402	2	2 Under GPU
	1 µF	X7R	0603	2	2 Under GPU
	4.7 µF	X6S	0603	2	2 Under GPU
	10 µF	X5R	0805	1	1 Near GPU
	22 µF	X5R	0805	1	1 Near GPU
GB4B-128 GDDR5	0.1 µF	X7R	0402	4	4 Under GPU
	1 µF	X7R	0603	4	4 Under GPU
	4.7 µF	X6S	0603	4	4 Under GPU
	10 µF	X5R	0805	2	2 Near GPU
	22 µF	X5R	0805	2	2 Near GPU
GB3-256 GDDR5	0.1 µF	X7R	0402	8	8 Under GPU
	1 µF	X7R	0402	14	14 Under GPU
	4.7 µF	X6S	0603	10	10 Under GPU
	10 µF	X5R	0805	6	6 Near GPU
	22 µF	X5R	0805	6	6 Near GPU

Notes:
1. At least two GND vias and two Power vias for each capacitor. All values in this table are preliminary; final values may change.
2. If a single partition 64-bit GPU is the GB4B-128 package is used, populate only half of the recommended number of decoupling capacitors of GB4B-128.

Table 3-14. FBx_PLL_AVDD and FB_DLL_AVDD Filtering

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU
GB4B-128	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	3 (1 per ball)	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU
GB3-256	FBx_PLL_AVDD	0.1 µF	X7R	0402	4 (1 per ball)	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

Note: Filtering for FB_PLL_DLL_AVDD on GB3-256 is combined with PLL filtering in section 3.9.2.

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Table 3-32. GB2B-64 and GB4B-128 PLLVDD Filtering

GPU Package	PLL Rail	Capacitor Type		Footprint	Population	Location
GB2B-64 and GB4B-128	PLLVDD	0.1 µF	X7R	0402	1	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.05)		0402	1	Near GPU

Table 3-33. SP_PLLVDD and VID_PLLVDD Power Rail Filtering Combined

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2B-64 GB4B-128 GB3-256	SP_PLLVDD + VID_PLLVDD	0.1 µF	X7R	0402	1 per ball	Under GPU
		4.7 µF	X5R	0603	1	Near GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		180 Ω (ESR=0.2)		0603	1	Near GPU

20140423

Follow N15x GPU design guide and implement OVERT function

GPIO13	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3_AON

DDR3	1.5V/ 1.5V	Single Rank						
			Hynix	H5TC4G63AFR-11C	A-die	0x0	1000	H/A	Production candidate
			Micron	MT41J256M16HA-093G:E	E-die	0x1	1000	1322	Production candidate
			Samsung	K4W4G1646D-BC1A	D-die	0x2	1000	H/A	Post-production candidate

Table 113. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND	
4.99 k	1000	0000	Hynix
10.0 k	1001	0001	
15.0 k	1010	0010	Samsung
20.0 k	1011	0011	
24.9 k	1100	0100	
30.1 k	1101	0101	
34.8 k	1110	0110	
45.3 k	1111	0111	

4.99Kohm	64.49915.6DL
10Kohm	64.10025.L0L
15Kohm	64.15025.6DL
20Kohm	64.20025.6DL
24.9Kohm	64.24925.6DL
30.1Kohm	64.30125.6DL
34.8Kohm	64.34825.6DL
45Kohm	64.45325.6DL

Table 15-3. GB2B-64 and GB4B-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AOH and pull-down to GND and stuff 50kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AOH and pull-down to GND for forward compatibility.			

Check with NV/ Ken

Hynix	H5TC4G63AFR-11C	A-die	0x0	1000
Micron	MT41J256M16HA-093G:E	E-die	0x1	1000
Samsung	K4W4G1646D-BC1A	D-die	0x2	1000

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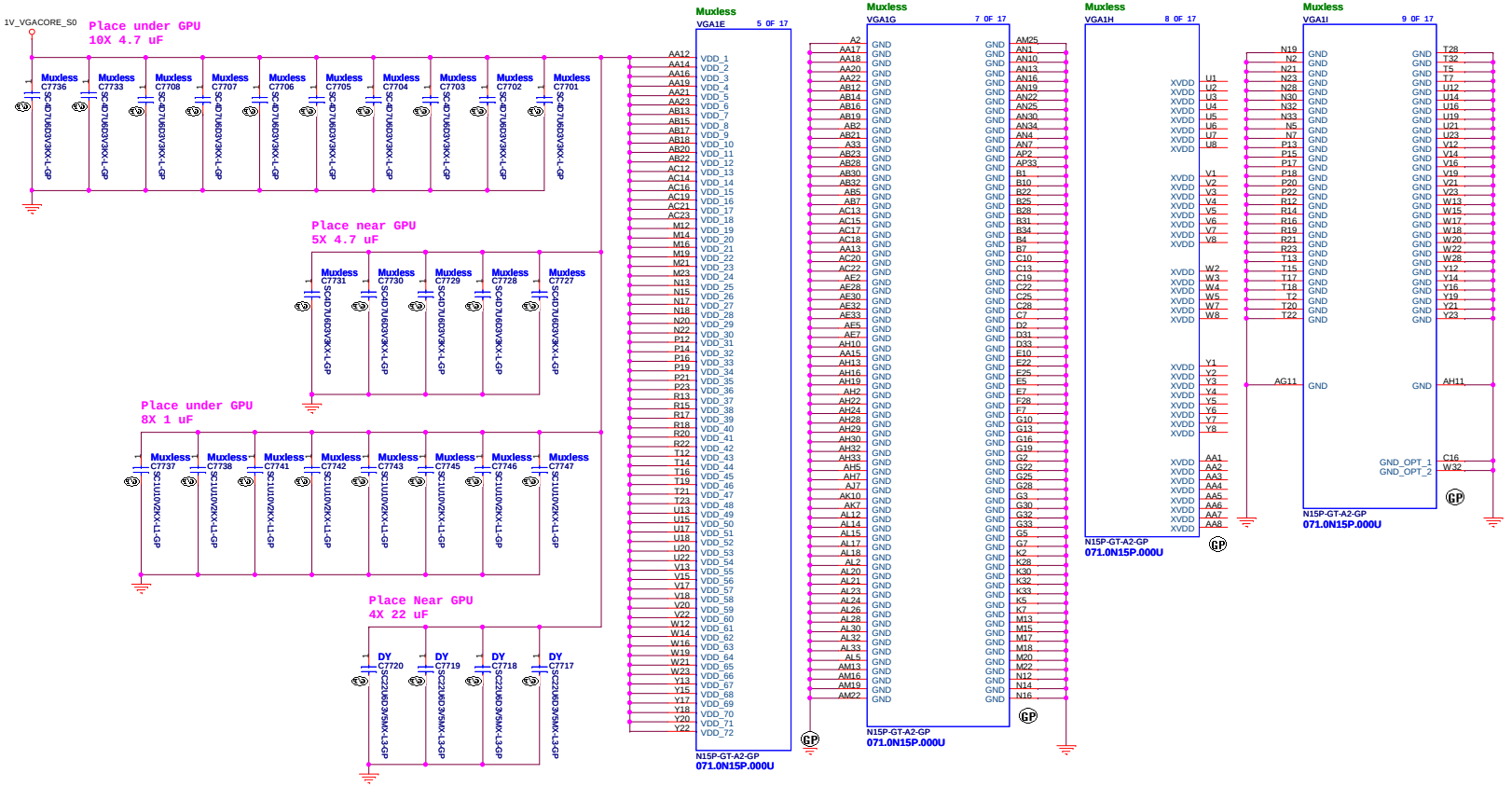

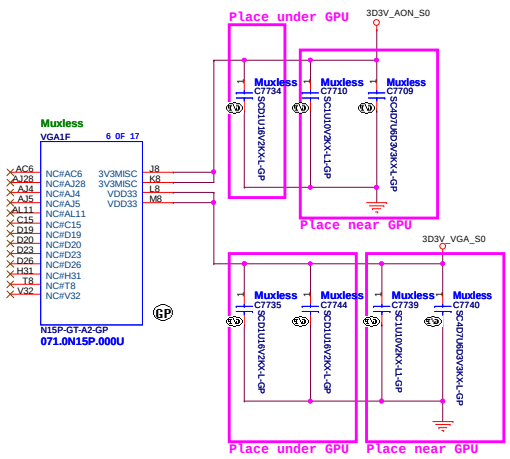

Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ
GB4B-128	4.7 µF	X6S	0603	15	15	Under GPU	
	1 µF	X6S	0402	8	8	Under GPU	
	22 µF	X5R	0805	14	7	Near GPU	See Note 2
	4.7 µF				5	Near GPU	
	330 µF	POS	7343	2	2	Near GPU	ESR ≤ 6 mΩ
GB3-256	0.1 µF	X7R	0402	20	20	Under GPU	
	4.7 µF	X6S	0603	40	40	Under GPU	
	10 µF	X5R	0805	4	4	Near GPU	
	22 µF	X5R	0805	11	11	Near GPU	
	100 µF	X5R	1206	4	0	Near GPU	
	330 µF	POS	7343	4	4	Near GPU	ESR ≤ 6 mΩ

Notes:
1. Generally the decoupling capacitor footprint requirement will remain the same but the population may get updated or may differ per GPU SKU. Always refer to the latest PUH for any NVVDD decoupling requirement update for specific GPU SKUs.
2. Combine / co-layout two 0805 footprints into each of the POSCAP footprint. So a total of four 0805 footprints should be placed inside the two POSCAP foot prints, allocating fourteen 0805 footprints total.

Table 3-27. 3.3V Power Rail Decoupling

GPU Package	Rail	Capacitor Type	Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.

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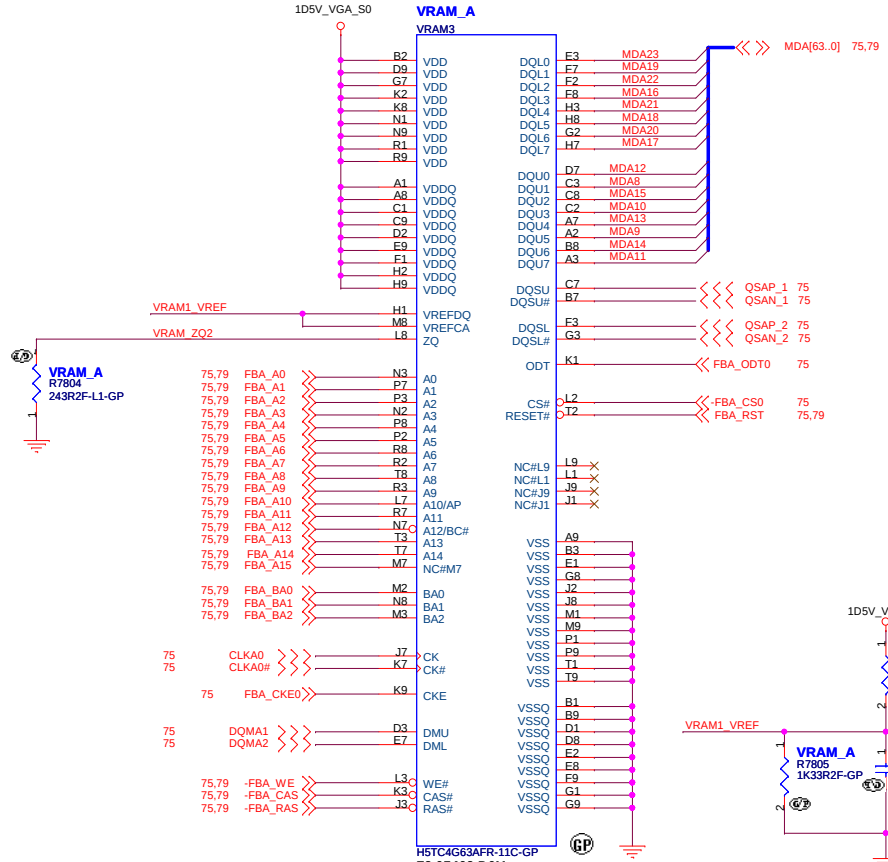
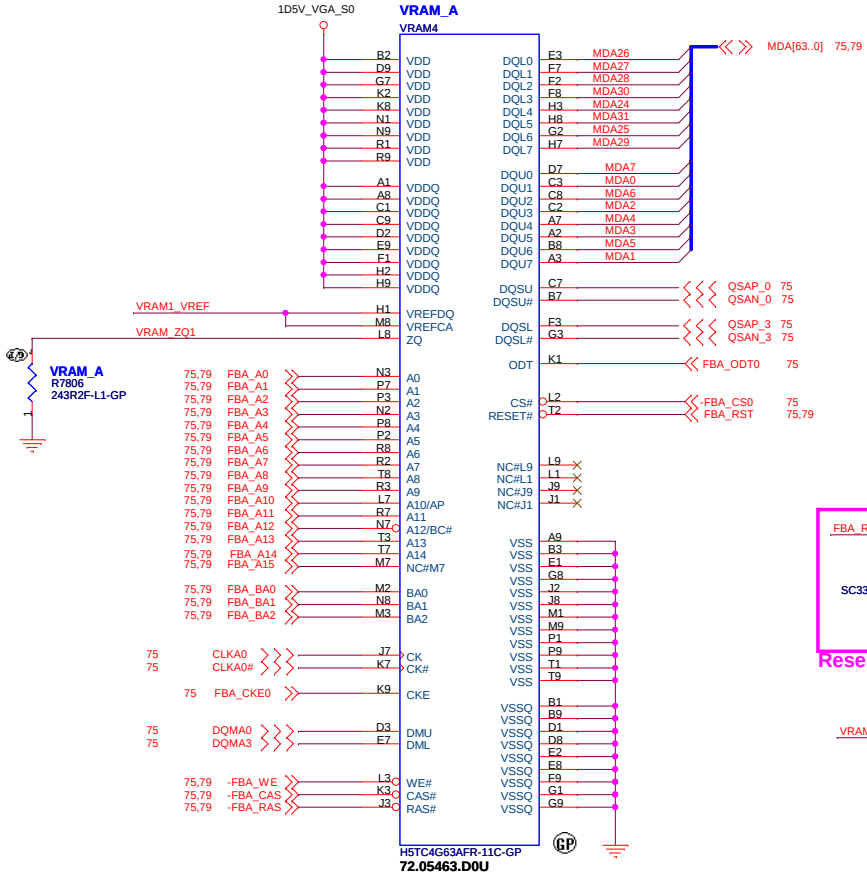
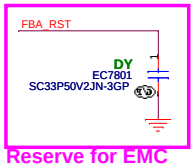
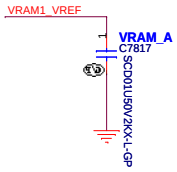
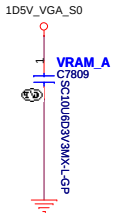










FOR VRAM3

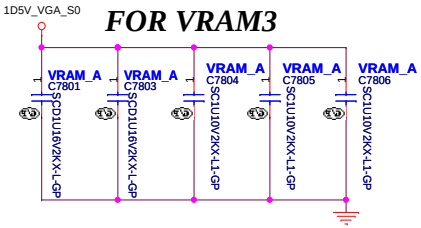
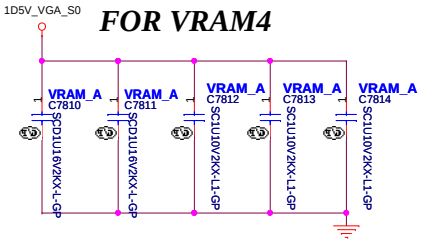


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

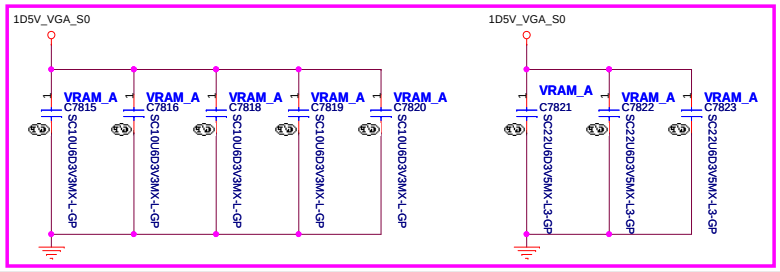
Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.



FOR VRAM4

0214/02/27



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Title: GPU-VRAM1,2 (1/4)

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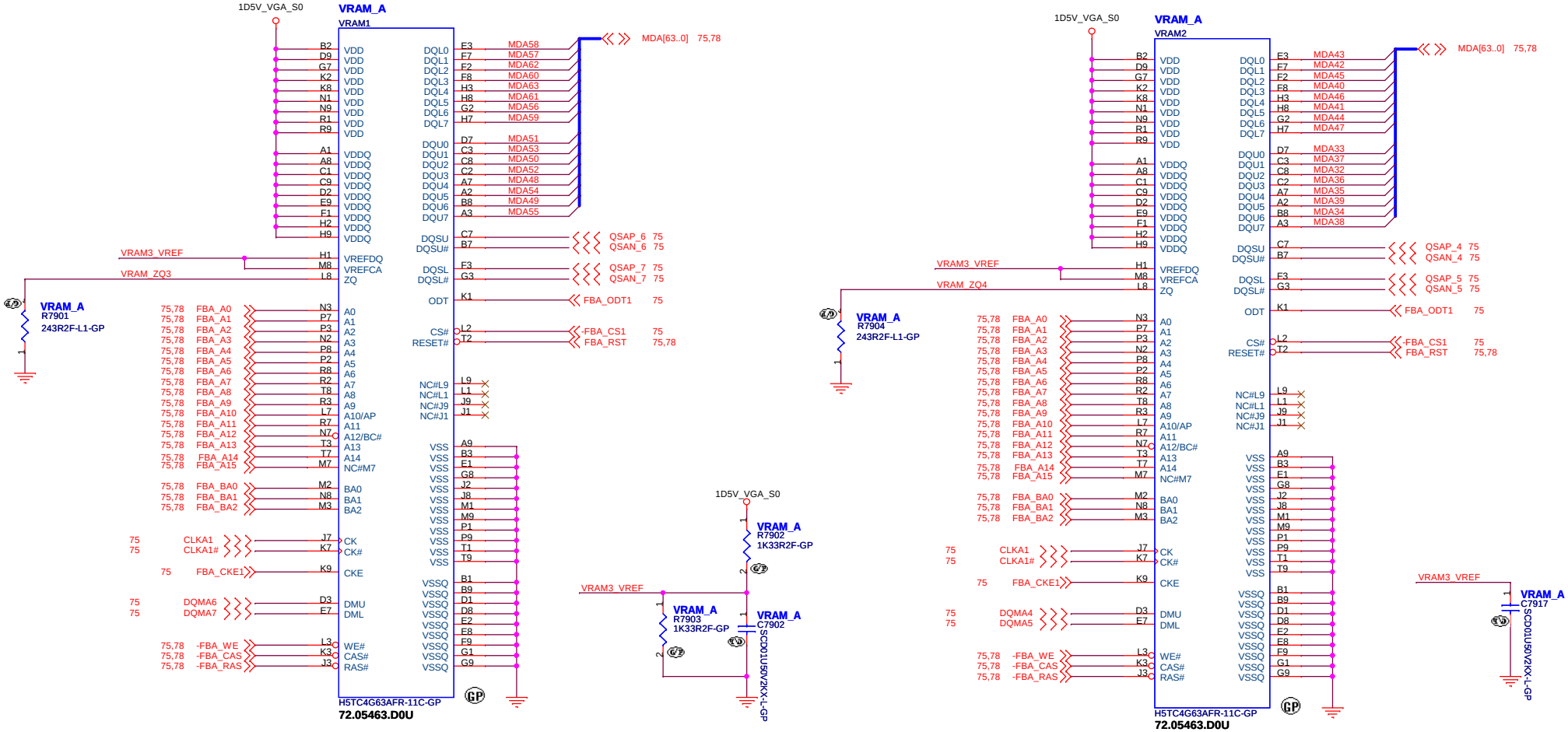
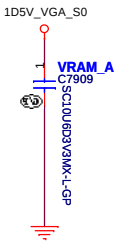




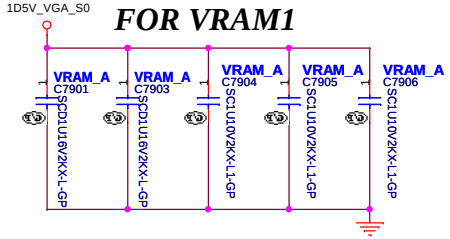
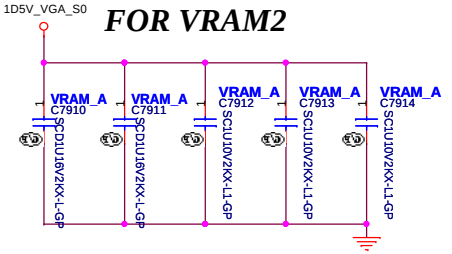


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.



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Title: **GPU-VRAM3,4 (2/4)**

Size	Document Number	Rev
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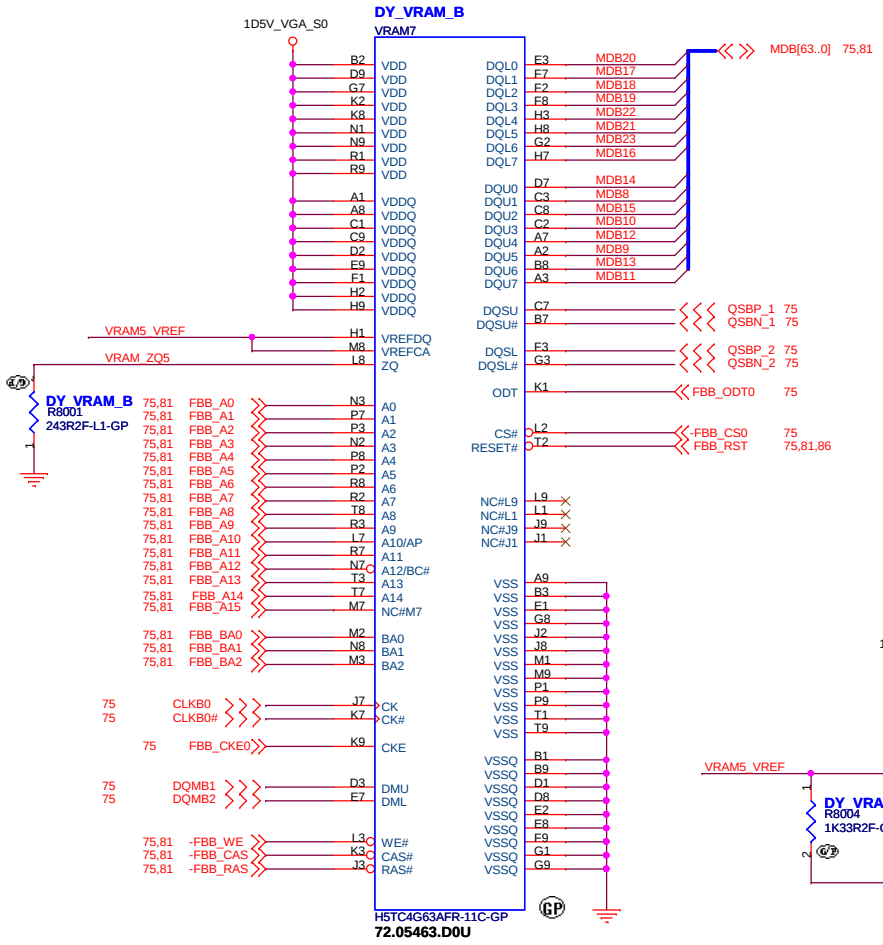
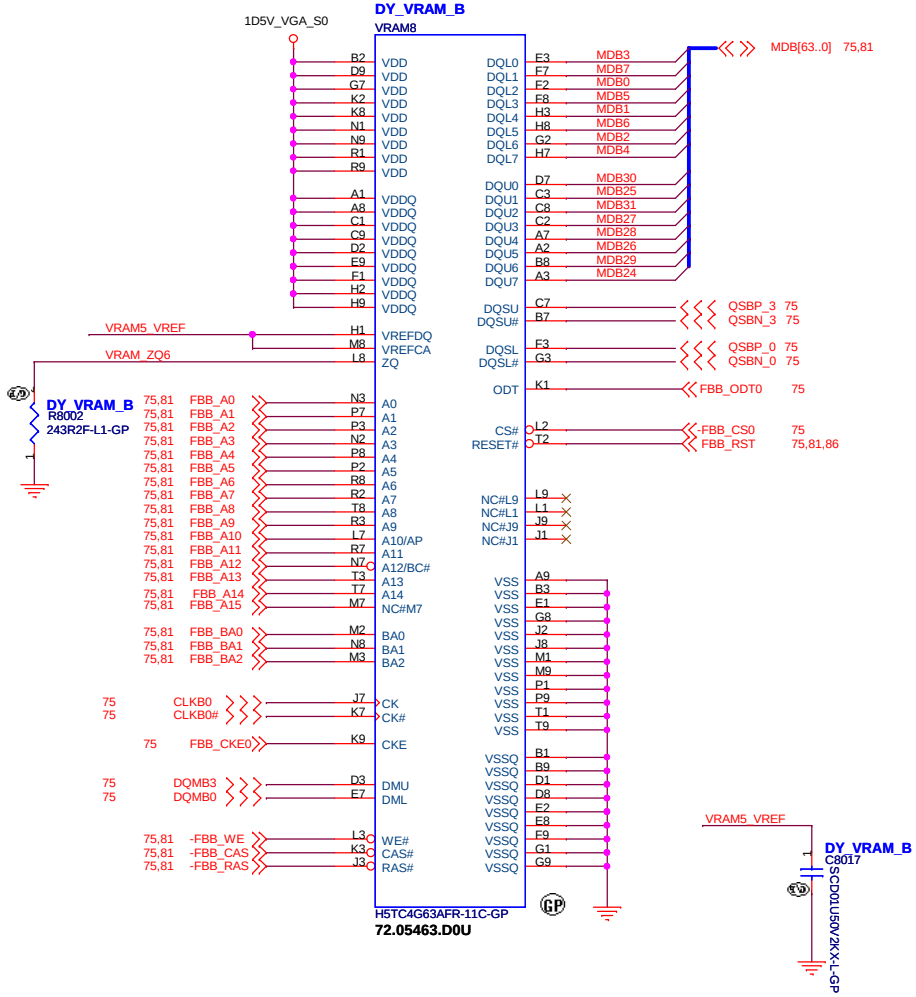




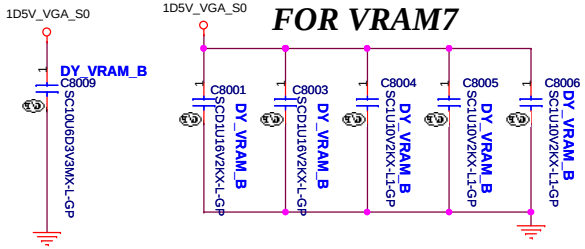
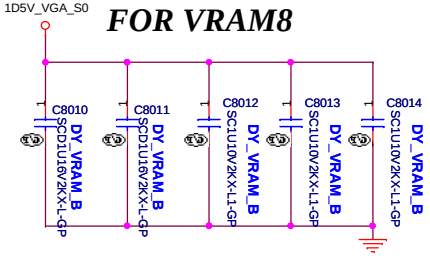


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separato					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.



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Title: **GPU-VRAM5,6 (3/4)**

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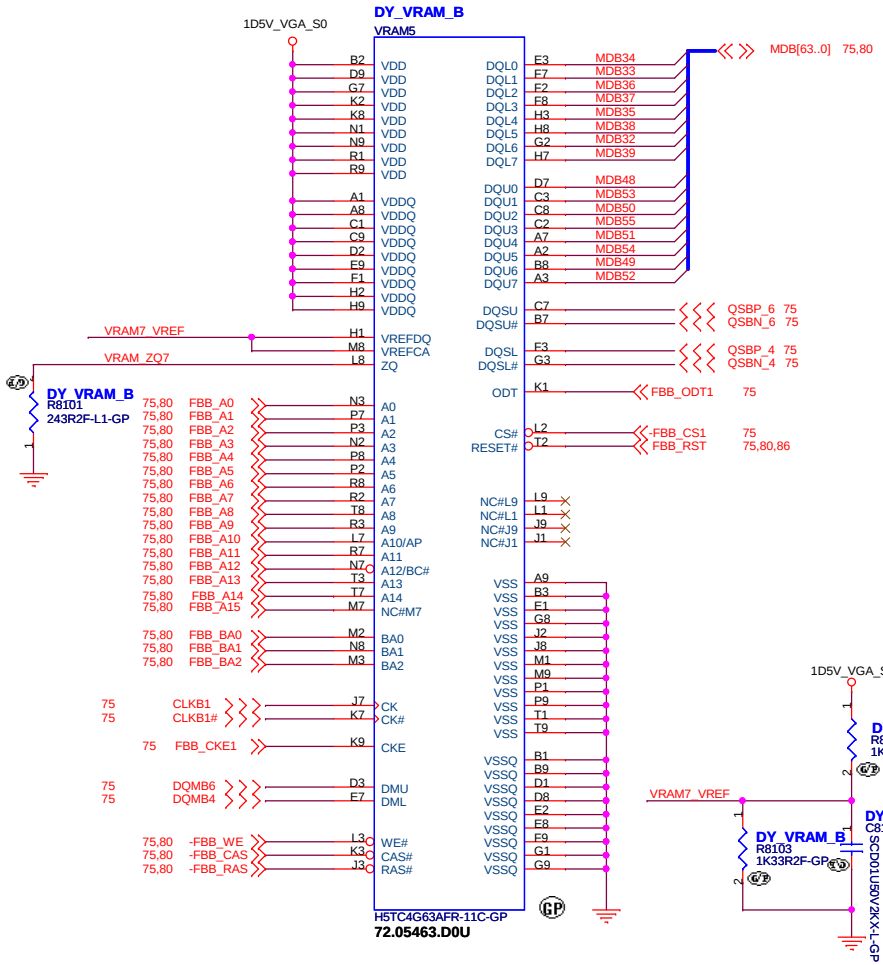
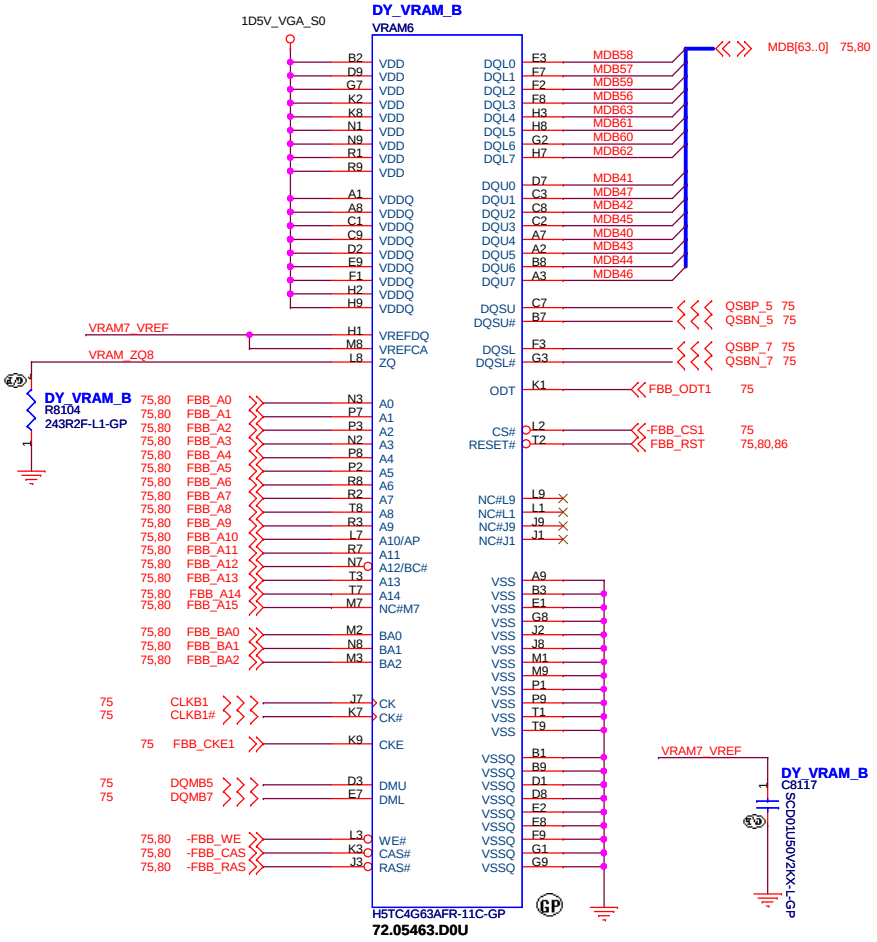
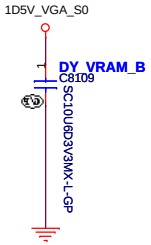
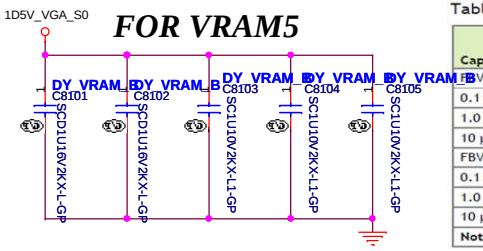






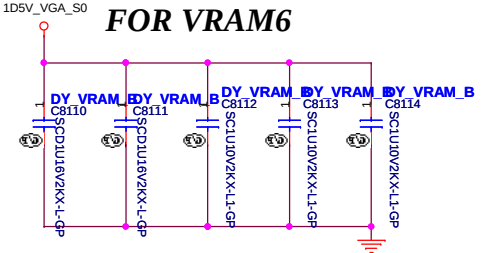


FOR VRAM5

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population		Location
			FBVDDQ	FBVDD	
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.



FOR VRAM6

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Title: **GPU-VRAM7,8 (4/4)**

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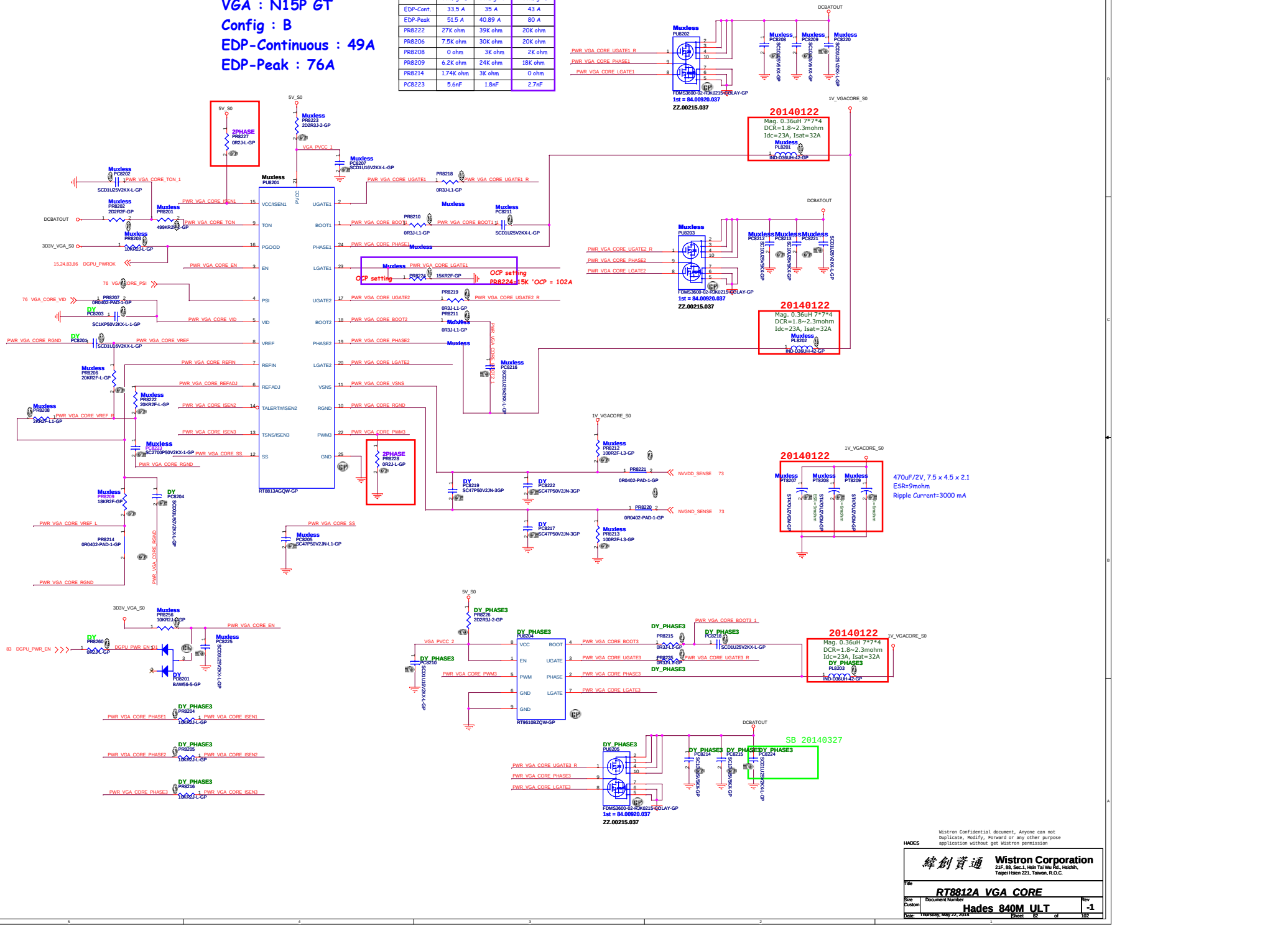
VGA : N15P GT
Config : B
EDP-Continuous : 49A
EDP-Peak : 76A

	Config : D	Config : C	Config : B
EDP-Cont.	33.5 A	35 A	43 A
EDP-Peak	51.5 A	40.89 A	80 A
PR8222	27K ohm	39K ohm	20K ohm
PR8206	7.5K ohm	30K ohm	20K ohm
PR8208	0 ohm	3K ohm	2K ohm
PR8209	6.2K ohm	24K ohm	18K ohm
PR8214	1.74K ohm	3K ohm	0 ohm
PC8223	5.6nF	1.8nF	2.7nF



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Title: RT8812A VGA CORE

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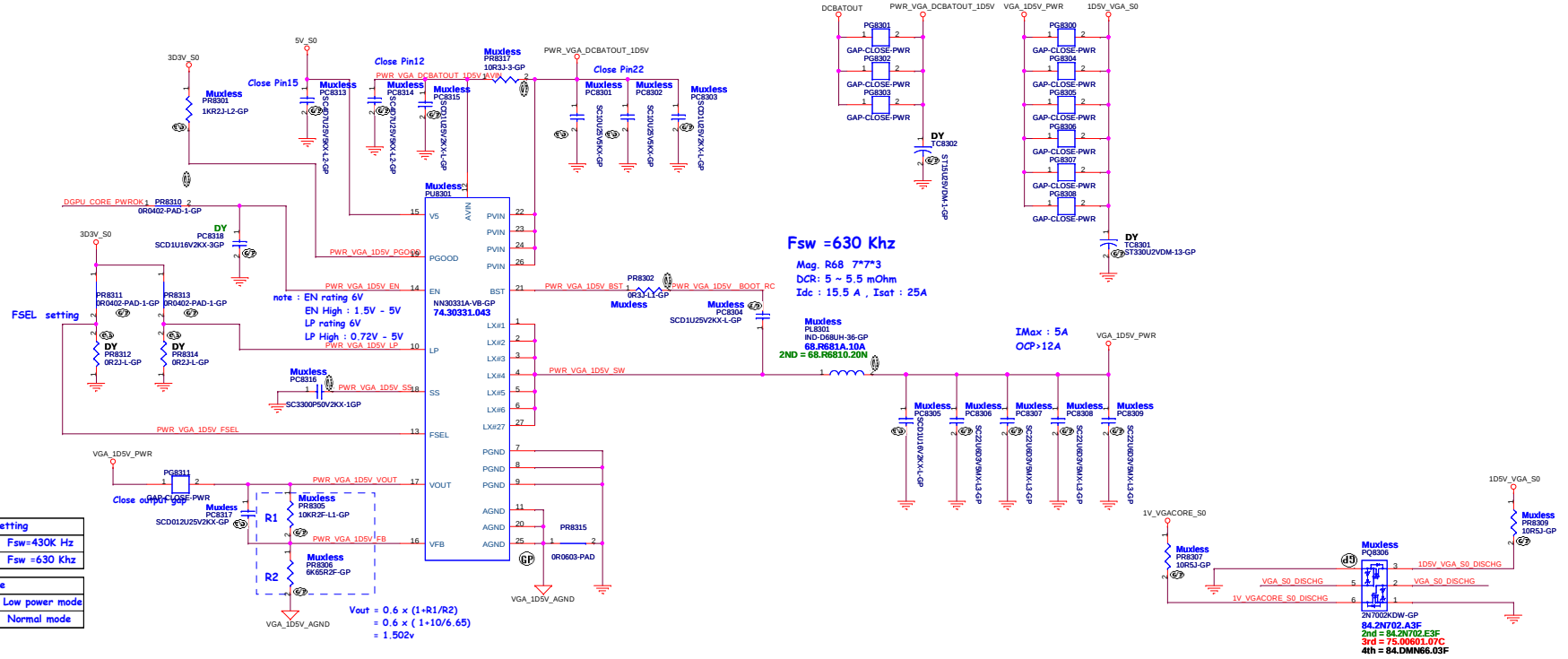
NN30331A for VGA_1D5V(For VRAM DDR3)

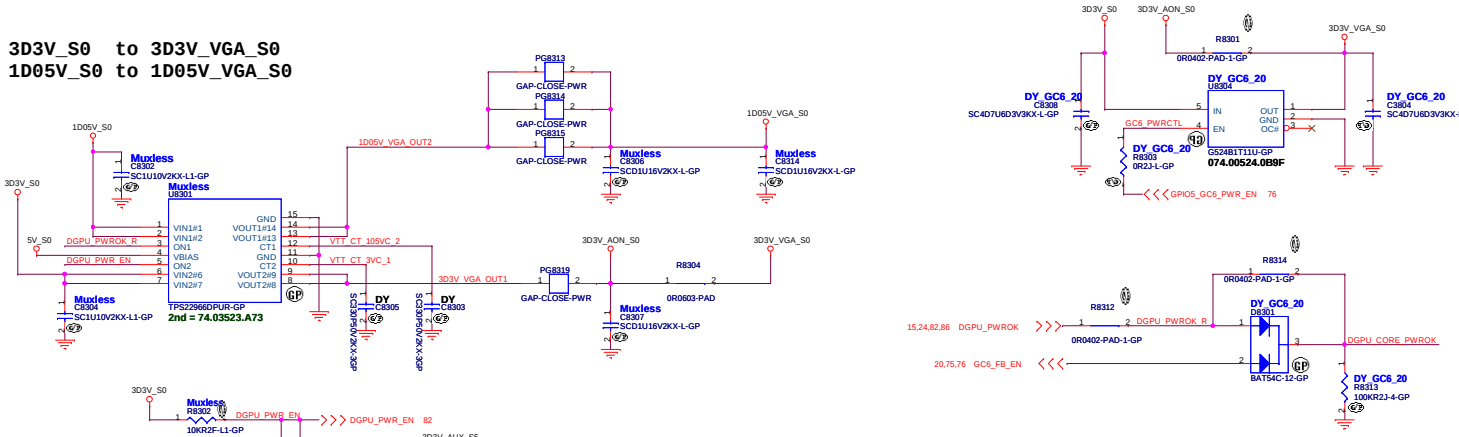
VGA_CORE&1D05V_VGA_S0 Discharge Circuit



FSEL setting	
	Fsw=430K Hz
High	Fsw =630 Khz

LP mode	
LOW	Low power mode
High	Normal mode

3D3V_S0 to 3D3V_VGA_S0
1D05V_S0 to 1D05V_VGA_S0



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Title: DISCRETE VGA POWER

Size	Document Number	Rev
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Switchable GFX LCD(1/2)

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Title

Switchable GFX LCD(2/2)

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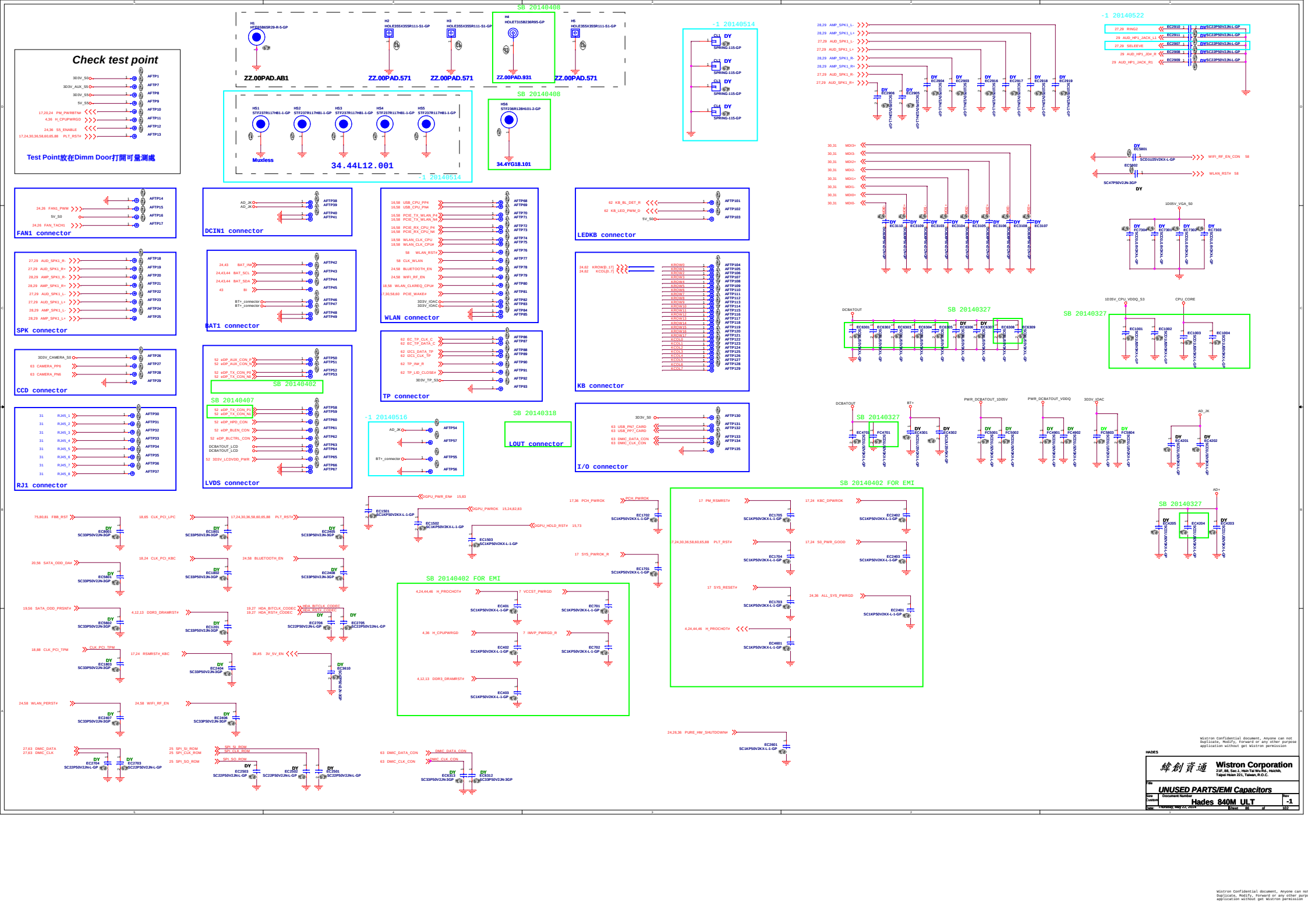
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Test Point放在Dimm Door打開可量測處
FAN1 connector
SPK connector
CCD connector
RJ1 connector
DCIN1 connector
BAT1 connector
LVDS connector
SB 20140402
SB 20140407
-1 20140516
TP connector
WLAN connector
LEDKB connector
KB connector
SB 20140318
LOUT connector
I/O connector
SB 20140408
Muxless
34.44L12.001
34.4YG18.101
-1 20140514
SB 20140327
SB 20140402 FOR EMI
-1 20140522
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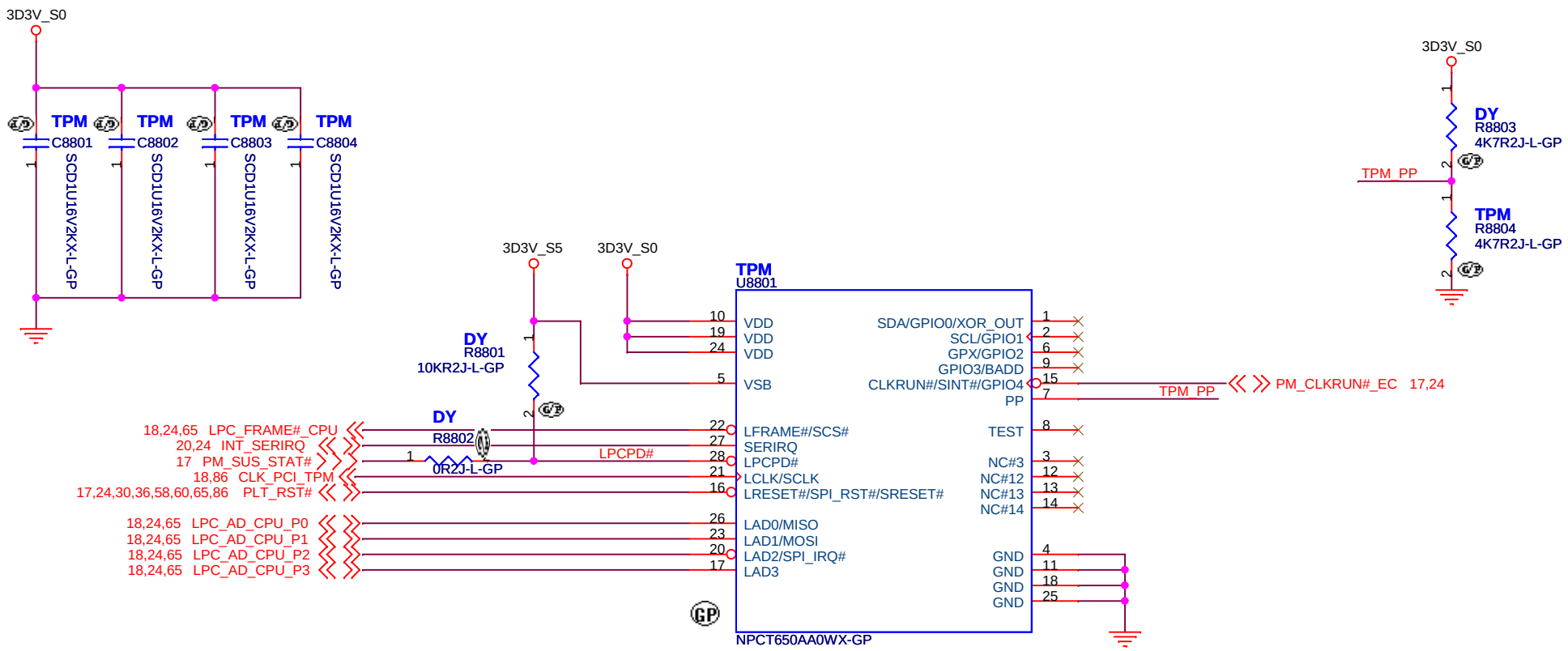

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Express Card

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Smart Card socket

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Switchable GFX eDP

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Title

Bottom Docking

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Title

Inter LAN WG1217LM

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LAN Switch

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A4	**Hades_840M_ULT**	**-1**

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Title

PCH_XDP

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Title

Change History

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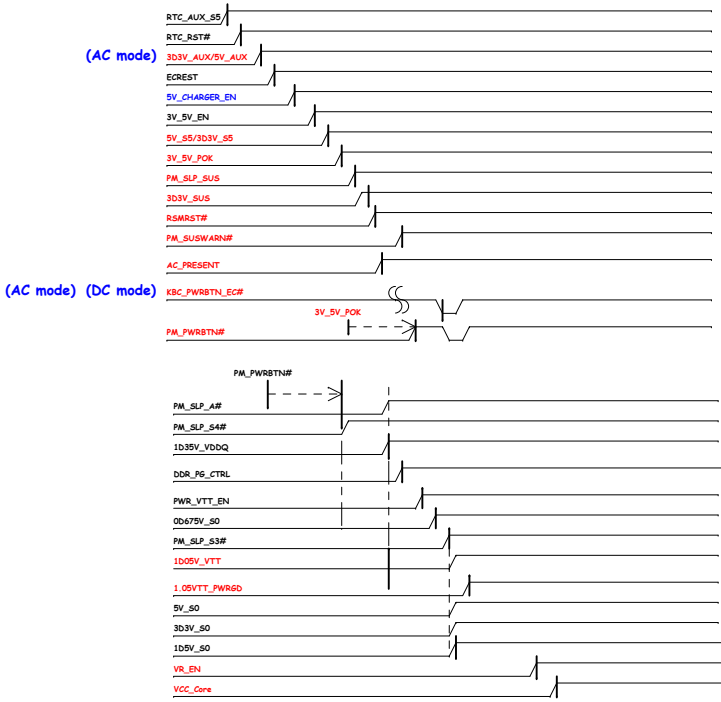
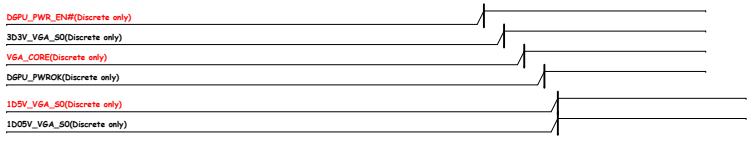
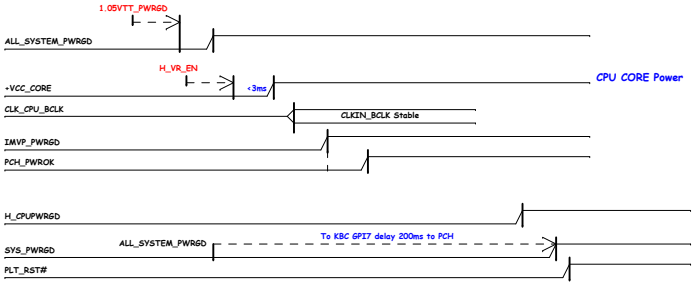
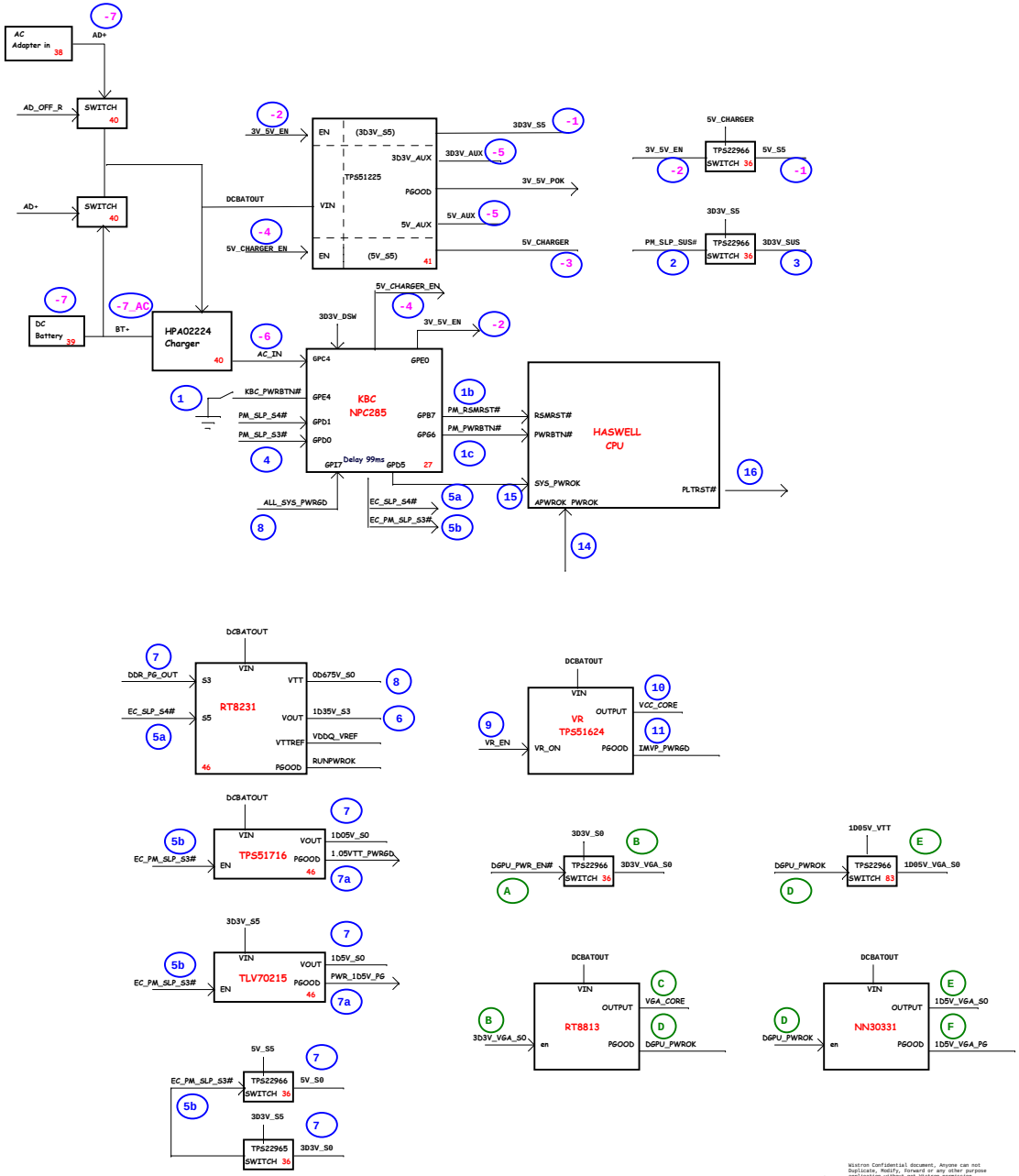
Intel-Power Up Sequence







HASWELL POWER UP SEQUENCE DIAGRAM



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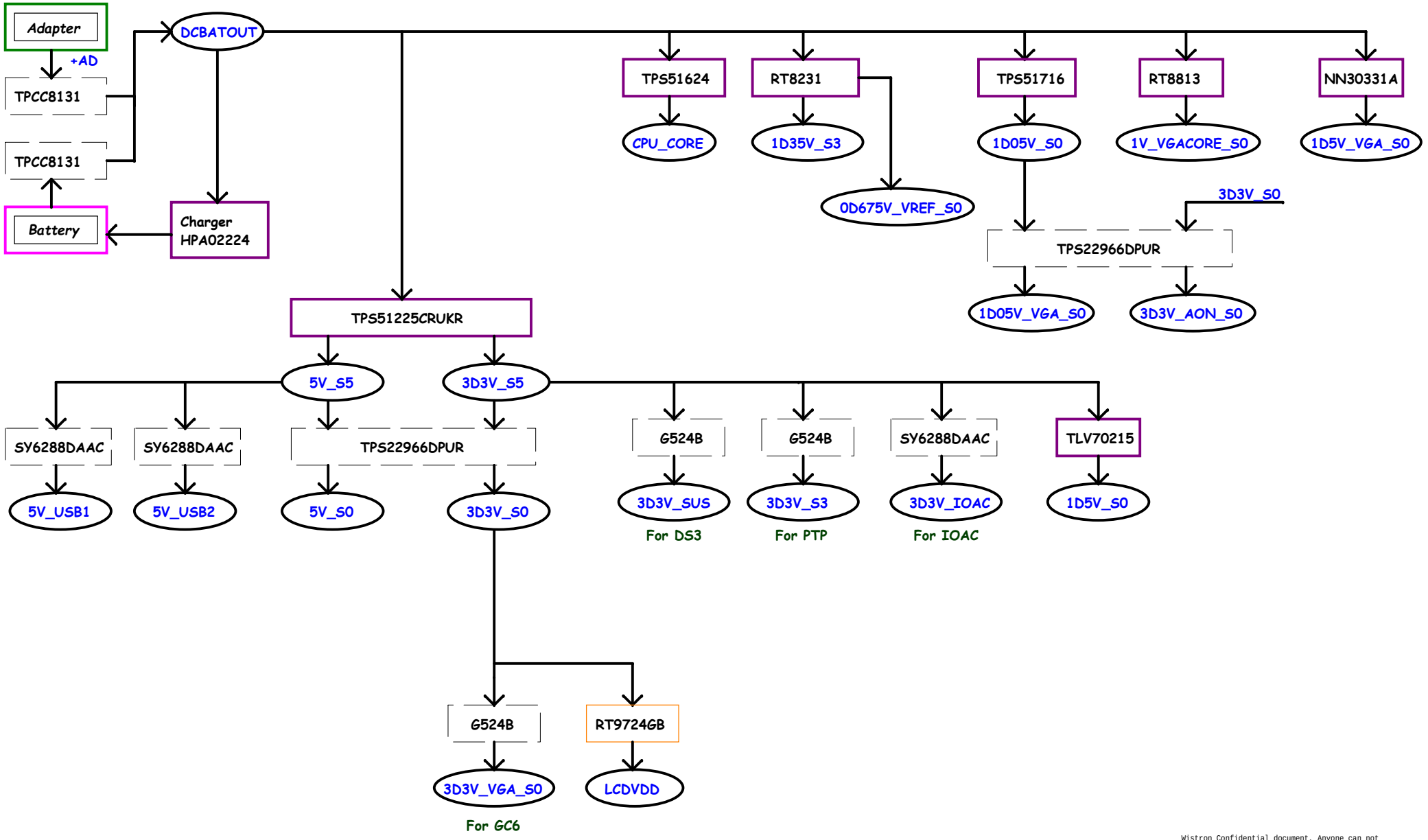

Power Shape

Regulator | LDO | Switch

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Title: Power Block Diagram

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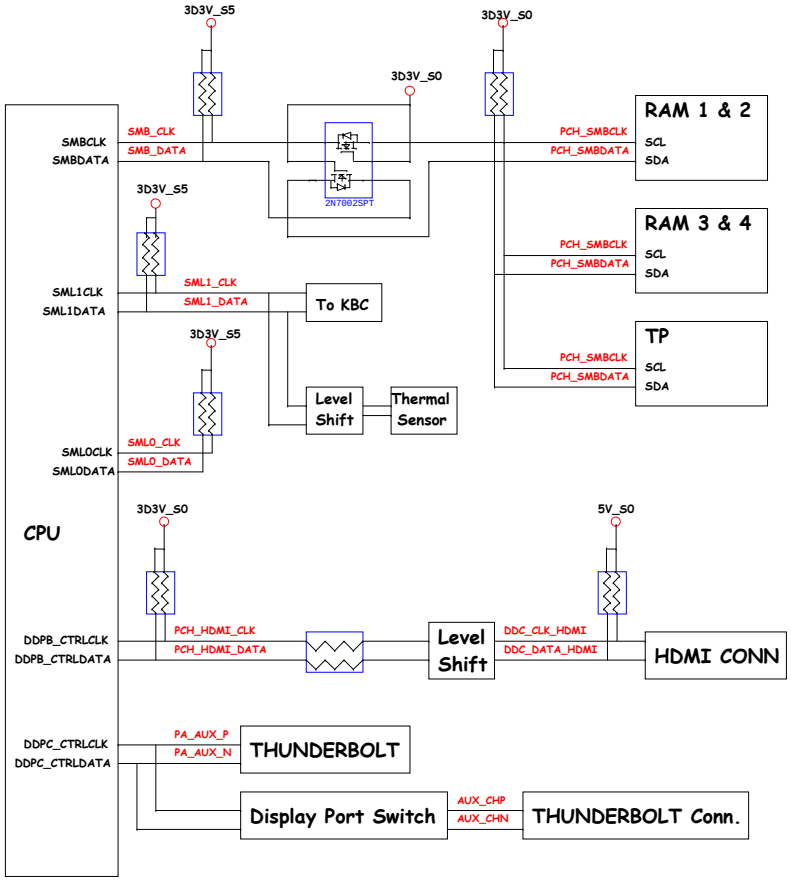
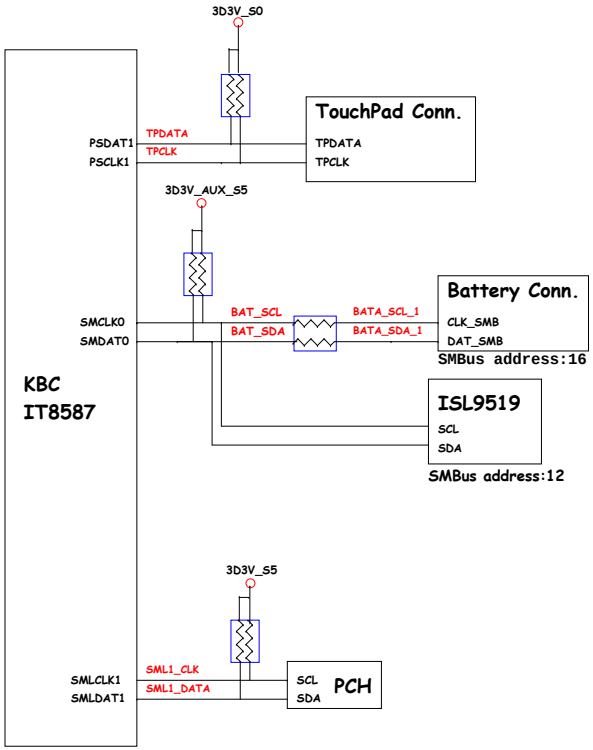
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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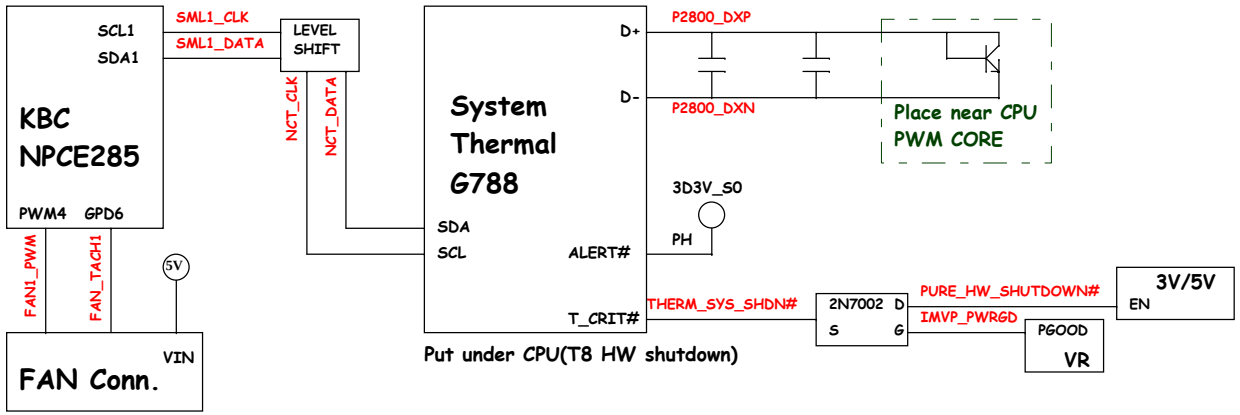
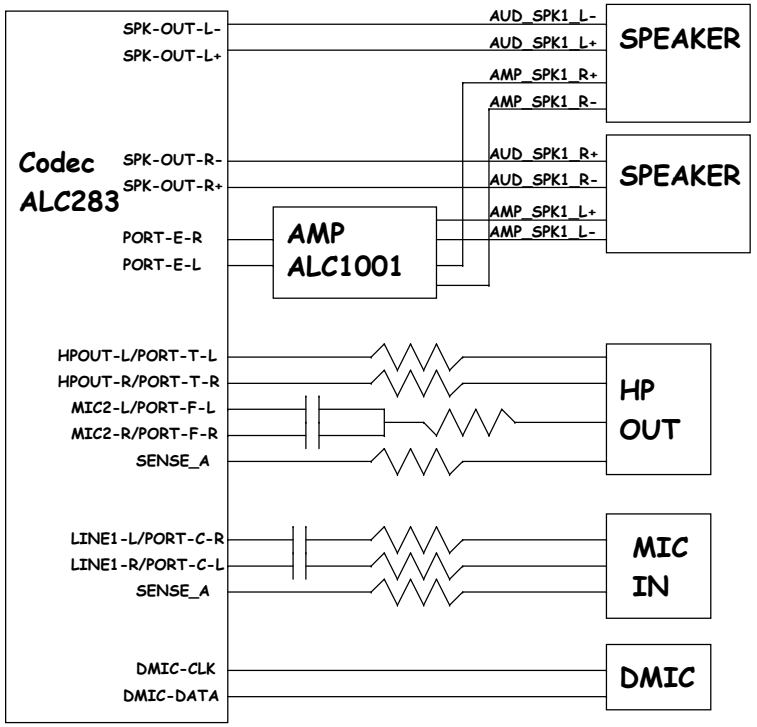
Thermal Block Diagram



Audio Block Diagram



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Title: **THERMAL/AUDIO BLOCK DIAGRAM**

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